Briefs

Electrothermal Characteristics of Strained-Si MOSFETs in High-Current Operation

Chang-Hoon Choi, Jung-Hoon Chun, and Robert W. Dutton

***Abstract*—Electrothermal characteristics of strained-Si MOSFETs, operating in the high-current regime have been studied using device simulation. The phonon mean-free-path of strained-Si devices in the presence of high electric fields is determined based on fullband Monte Carlo device simulation. Strained-Si nMOS devices have higher bipolar current gain and impact ionization rates compared to bulk-Si nMOS devices due to the smaller energy bandgap and longer phonon mean-free-path. Even though strained-Si devices have self-heating problems due to the lower thermal conductivity of the buried SiGe layer, the devices can be used beneficially for electrostatic discharge protection devices to achieve lower holding voltage (V_h) and higher second breakdown triggering current (I_{t2}), compared to those of bulk-Si devices, owing to the high bipolar current gain and current uniformity.**

***Index Terms*—Bipolar current gain, device simulation, electrostatic discharge (ESD), fullband Monte Carlo simulation, phonon mean-free-path, self-heating problem, SiGe, strained-Si MOS.**

I. Introduction

Strained-silicon has drawn attention due to its enhanced carrier transport and its compatibility with mainstream Si CMOS processing [1]. Carrier transport enhancement is made by enhanced carrier mobility in the epi-Si layer due to biaxial tensile stress that induces repopulation of the energy bands [2]. On the other hand, self-heating problems can cause performance degradation in strained-Si device, because the thermal conductivity of $Si_{0.8}Ge_{0.2}$ is ~ 15 times lower than that of bulk-Si [3], [4]. Thermal properties of transistors are critical, especially for electrostatic discharge (ESD) and other reliability problems. Thus, in order to realize strained-Si CMOS LSI, studying intrinsic electrothermal characteristics of strained-Si device is of technological importance. In this brief, electrical and thermal characteristics of strained-Si are compared with bulk-Si device by using device simulations with the phonon mean-free-path parameter determined from the full-band Monte Carlo analysis.

II. Modeling for Strained-Si Device

Fig. 1(a) shows the device structures of bulk nMOS and strained-Si nMOS; the strained-Si nMOS has a strained-Si layer of 15-nm thickness and source/drain junction depth of 50 nm. The gate length is 130 nm and the gate oxide thickness is 2.5 nm for both structures. The channel dopant concentration for both structures is about $1 \times 10^{18}/\mathrm{cm}^3$ in the presence of halo implantation.

In order to determine the energy band structure of the strained-Si devices, material parameters are used based on [5]. Fig. 1(b) shows energy band diagrams for strained- and bulk-Si devices based on MEDICI [6] simulations. Thus, impact of bi-axial tensial strain of SiGe is modeled by stress-induced bandgap changes. Bandgap and

Manuscript received January 19, 2004; revised July 9, 2004. This work was supported in part by the MARCO/DARPA Focus Center on Materials, Structures, and Devices, and in part by Texas Instruments. The review of this brief was arranged by Editor S. Kimura.

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Digital Object Identifier 10.1109/TED.2004.836542

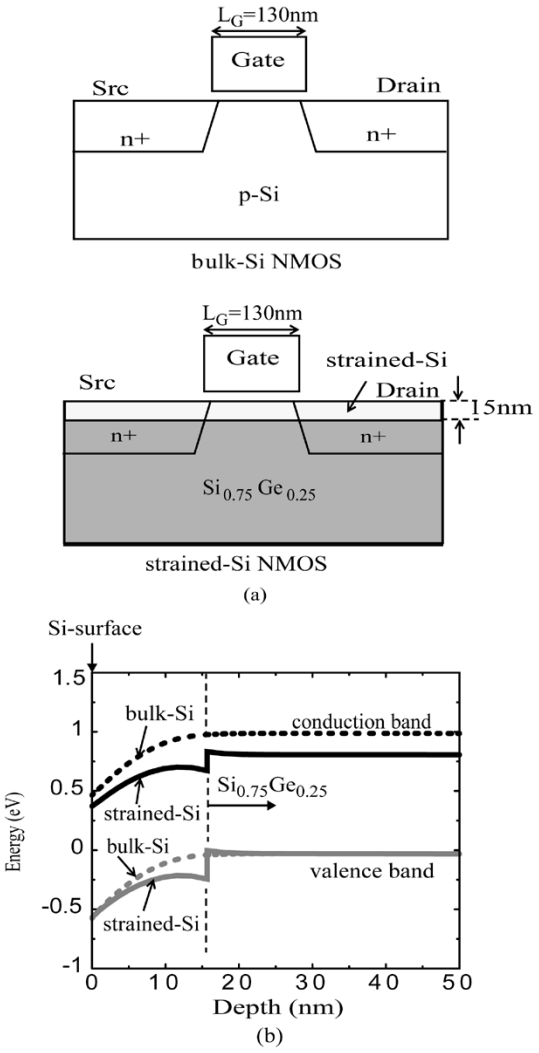

Fig. 1. Device structures and band diagrams for bulk- and strained-Si nMOS, (a) bulk-Si and strained-Si nMOS with 15 nm of strained-Si layer on $Si_{0.75}Ge_{0.25}$ layer, (b) simulated band-diagrams of the strained- and bulk-Si devices into the depth direction at $V_G = 0$ V.

permittivity of strained-Si layer $(E_{g,\mathrm{SSi}}, \epsilon_{r,\mathrm{SSi}})$ and relaxed $Si_{1-x}Ge_x$ layer $(E_{g,\mathrm{SiGe}}, \epsilon_{r,\mathrm{SiGe}})$ are defined according to [5]:

$$E_{g,\mathrm{SS}} = 1.08 - 0.4x \tag{1}$$

$$E_{g,\mathrm{SiGe}} = 1.08 - 0.729x \tag{2}$$

$$\epsilon_{r,\mathrm{SiGe}} = 11.8 + 4.2x \tag{3}$$

where x is the Ge mole fraction in the $Si_{1-x}Ge_x$, and the bandgap of Si is 1.08 eV at the room temperature. The simulated threshold voltages are 0.46 and 0.25 V for bulk-Si and strained-Si device, respectively. For simulation of drain current, temperature dependent carrier mobility [7], and temperature dependent bandgap models are employed to account for thermal effects.

The electron impact-ionization rate $(\alpha_{n,ii})$ for high current device operation is given as [6]

$$\alpha_{n,ii} = \alpha_{n,ii0} \cdot \exp\left[-\frac{E_g(T)}{q\lambda_n E_{n,\|}}\right] \tag{4}$$

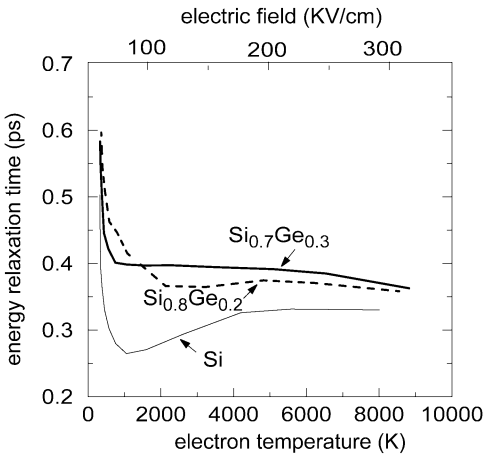

Fig. 2. Electron energy relaxation times with respect to electron temperatures and electric fields for strained- and bulk-Si calculated by using full-band Monte Carlo device simulation.

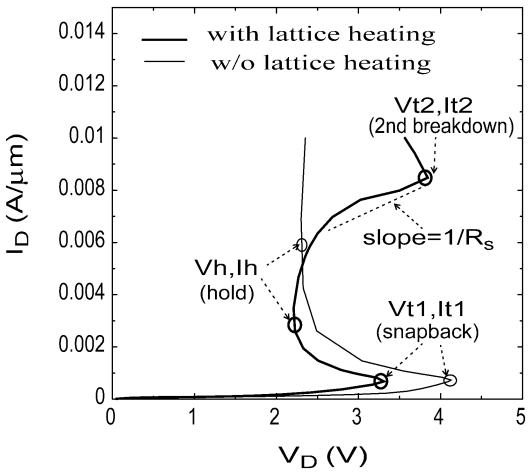

Fig. 3. Simulated I_D–V_D curves for the strained-Si nMOS represented in Fig. 1(a), with and without thermal effects (lattice heating model).

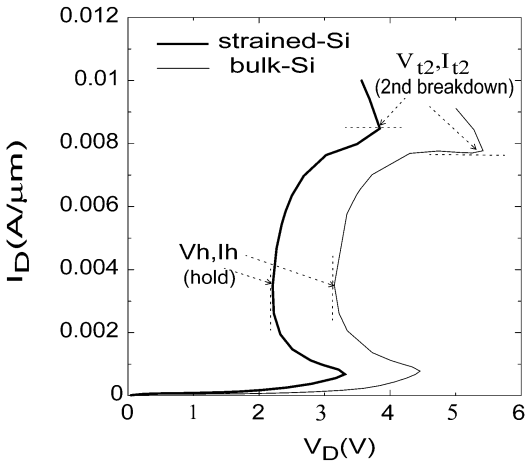

Fig. 4. Simulated I_D–V_D curves for strained-Si and bulk-Si nMOS. Thermal failure occurs for the bulk-Si device when the drain current is about ~ 0.01 A/μm.

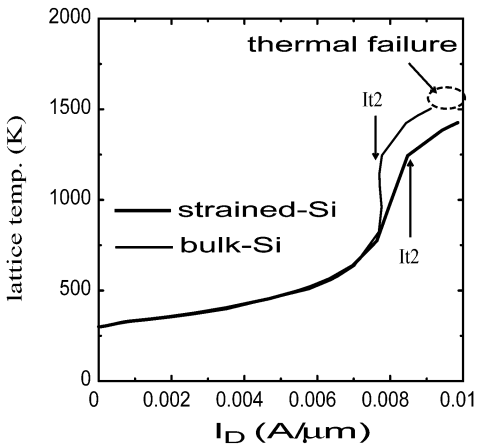

Fig. 5. Peak lattice temperatures with respect to the drain current for strained-Si and bulk-Si nMOS.

where $\alpha_{n,ii0}$ is a multiplicative factor of the electron ionization coefficient with a typical value of 7×10^5/cm and $E_{n,\|}$ is the electric field in the current flow direction. In order to determine the phonon mean free path of electrons (λ_n) for strained-Si, the energy relaxation times are calculated, since the mean free path is closely related to the energy relaxation times in scattering process [8]. Fig. 2 represents the calculated energy relaxation times for electrons in strained-Si and bulk-Si with respect to electric field and electron temperature, based on full-band Monte Carlo (FBMC) device simulations [9]. In the [1] the energy relaxation time was increased by roughly a factor of two from the bulk-Si value. The FBMC simulation results in Fig. 2 show that the increase of energy relaxation time of the strained-Si, relative to bulk-Si, is reduced as the electric field increases (i.e., at high electron temperatures). This implies that the mean-free-path (λ_n) in strained-Si for high current operation should be reduced from that used in the lower electric field regime. For an electric field of 300 KV/cm ($\simeq 8000$ K electron temperature), the energy relaxation times are 0.37, 0.36 and 0.33 ps for $Si_{0.7}Ge_{0.3}$, $Si_{0.8}Ge_{0.2}$ and bulk-Si, respectively. In this brief, λ_n of the strained-Si on $Si_{0.75}Ge_{0.25}$ layer has been assumed to increase by 20% from that for the bulk-Si—$\lambda_n = 10$ nm for bulk-Si and $\lambda_n = 12$ nm for strained-Si on $Si_{0.75}Ge_{0.25}$ at the temperature of 300 K.

III. Electro-Thermal Device Simulation

Electro-thermal device simulations are performed by using MEDICI for strained- and unstrained-Si (bulk) devices based on the previously determined material parameters. Fig. 3 shows simulated I_D–V_D curves for the strained-Si devices represented in Fig. 1(a), both with and without the inclusion of thermal effects. The snapback voltage (V_{t1}), which triggers the parasitic n-p-n transistor in a self-biasing mode, for the strained-Si device becomes lower when thermal effects are considered. This is due to the reduced bandgap and increased density of states as the lattice temperature is increased. As the current rises above the snapback current (I_{t1}), the lattice temperature rises significantly, which results in reduced carrier mobility and increased series resistance (R_s). As the current increases further, the bandgap is reduced significantly which triggers the second breakdown (V_{t2} and I_{t2}) at $V_D \sim 4$ V. Second breakdown is generally considered to be caused by current localization due to the negative resistance coefficient of silicon when the thermally generated carrier concentration is equal to the background doping concentration. This results in irreversible thermal damage to the device beyond the critical temperature (T_c) [10]. Fig. 3 shows that second breakdown is not observed without consideration of the thermal effects.

Fig. 4 shows simulated I_D–V_D curves for strained- and bulk-Si devices ($V_G = 0$ V). The impact ionization rate $(\alpha_{n,ii})$ and the current gain of the parasitic bipolar (β) in the strained-Si are expected to be higher than those for bulk-Si devices due to the reduced bandgap and effects of carrier-to-carrier scattering. $\alpha_{n,ii}$ values for strained-Si and

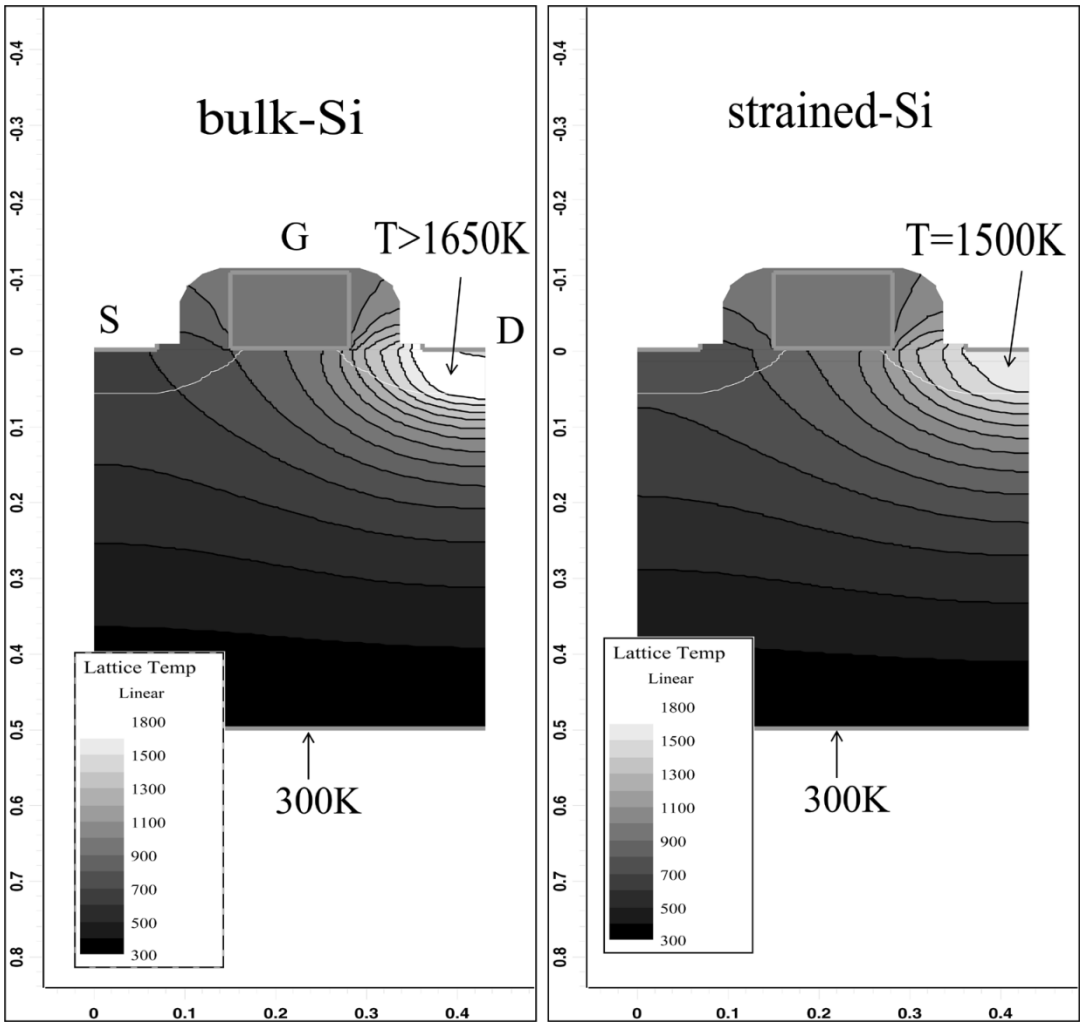

Fig. 6. Temperature contours for bulk-Si (left-hand) and strained-Si (right-hand) devices at $I_D = 0.01\ \mathrm{A}/\mu\mathrm{m}$.

SiGe layers are higher than that for bulk-Si by $\sim 20\%$ and 30%, respectively, estimated from (3), assuming the E_g and λ_n parameters discussed in Section II. The current gain (β) of S-Si device, considering only for bandgap reduction is $\sim 10\%$ higher than bulk-Si, simply based on $\beta \propto \exp(\Delta E_g/kT)$ relationship. This β will be even higher if increased $\alpha_{n,ii}$'s of strained-Si and SiGe are taken into account during the parasitic bipolar action.

From an ESD perspective, a protection device with a high bipolar current gain (β) is advantageous for discharging current, according to the pioneering work in SiGe technology [11], [12]. The snapback voltage of the strained-Si device is lower by 1 V than that for the bulk-Si device. The hold voltage (V_h), the minimum voltage required for the bipolar operation, is also lower for the strained-Si device. The second breakdown triggering current (I_{t2}) for strained-Si devices is higher by $\sim 10\%$ relative to bulk-Si devices. As a result, the power density and peak lattice temperature during parasitic bipolar operation are lower for the strained-Si device than that for the bulk-Si device. In addition, once the parasitic bipolar turns on, uniform conduction can be achieved in the strained-Si device, in which current flows mainly through the buried SiGe layer rather than through the surface layer, which can suppress current localization at the Si surface. In other words, the main current path is the strained-Si layer during normal operation, while the main current path during the parasitic bipolar action is the buried SiGe layer.

Fig. 5 shows the peak temperature versus drain current (I_D) for bulk- and strained-Si devices. There is an abrupt increase of lattice temperature at $\sim 0.008\ \mathrm{A}/\mu\mathrm{m}$ of drain current for the bulk-Si device. As a result, thermal failure occurs for the bulk-Si device when the drain current is $\sim 0.01\ \mathrm{A}/\mu\mathrm{m}$ (I_{t2}) due to its high power density. This implies that even though the thermal dissipation of strained-Si is worse compared to silicon due to the 15 times lower thermal conductivity of SiGe layer, the local temperature overheating can effectively be suppressed in strained-Si devices owing to the higher bipolar gain (β) and current uniformity.

Fig. 6 shows temperature contours for bulk-Si and strained-Si devices at a drain current of $0.01\ \mathrm{A}/\mu\mathrm{m}$; temperature overheating is severer for bulk-Si at the surface near the drain region $(T > T_c \sim 1650\ ^\circ\mathrm{K})$, while the peak lattice temperature of the strained-Si device is lower than for bulk-Si $(\sim 1500\ ^\circ\mathrm{K})$ owing to its higher I_{t2} than that of the bulk-Si device.

One of the main factors affecting ESD failure in the protection device is nonsimultaneous triggering of multifinger gate transistors. This can be caused by asymmetries between the fingers due to the process variations and substrate resistance that produce RC delays for triggering adjacent fingers. Since a strained-Si transistor can shunt high levels of current, while maintaining low voltage and power consumption, it can eliminate the nonsimultaneous triggering problem in finger-type protection devices [13].

IV. Summary

Strained-Si–SiGe nMOS devices show higher bipolar current gain (β) and impact ionization rates compared to bulk-Si nMOS due to narrower energy bandgap and longer phonon mean-free-path. Even though the thermal dissipation of strained-Si/SiGe structure is worse compared to silicon due to the lower thermal conductivity of the buried SiGe layer, the local temperature overheating can effectively be suppressed in strained-Si devices owing to $\sim 20\%$ higher β and current uniformity, because the main current path during the parasitic bipolar action is the buried SiGe layer. Thus, the strained-Si nMOS can be used effectively for ESD protection devices, despite self-heating problems caused by the lower thermal conductivity of the SiGe layer.

Acknowledgment

The authors are grateful to Dr. C. Jungemann for the Monte Carlo device simulation.

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Investigation of the Four-Gate Action in G^4-FETs

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***Abstract*—The four-gate silicon-on-insulator transistor (G^4-FET) combines MOS and JFET actions in a single transistor to control the drain current. The various operation modes of the G^4-FET are analyzed based on the measured current–voltage, transconductance and threshold characteristics. The main parameters (threshold voltage, swing, mobility) are extracted and shown to be optimized for particular combinations of gate biasing. Numerical simulations are used to clarify the role of volume or interface conduction mechanisms. Besides excellent performance (such as subthreshold swing and transconductance) and unchallenged flexibility, the new device has the unique feature to allow *independent* switching by its four separate gates, which inspires many innovative applications.**

***Index Terms*—JFET, MOSFET, multiple-gate transistor, silicon-on-insulator (SOI).**

I. Introduction

The International Technology Roadmap for Semiconductors recommends not only switching from bulk to silicon-on-insulator (SOI), but also evolving from single-gate planar SOI transistors to multiple-gate devices [1] with improved current drive and short-channel characteristics. Several innovative SOI devices, like double-, triple-, and four-gate transistors have been demonstrated. However, in these devices, the term "multiple" generally represents the number of *channels* switched by one gate and not the number of gates. For example, the "tri-gate transistor" [2] has only one gate covering the three sides of the body which leads to the three conduction channels switched together.

We have recently proposed a genuine four-gate transistor (G^4-FET) [3]. The initial characteristics showed the possibility to *independently* bias its four gates [3]. This device can be manufactured using fully scalable conventional SOI processes, without necessitating additional fabrication steps. In this brief, we present new data and an advanced analysis of G^4-FET features and performance by revealing the main conduction and gate-coupling mechanisms. The device configuration is described in Section II. Systematic measurements, given in Section III, clarify the role of each gate as well as the bias conditions for which one gate has maximum impact on the current modulation. The key parameters (drain current, subthreshold swing, threshold voltage, transconductance) corresponding to each *active* gate are extracted as a function of the *passive* gates biases. Their variations are explained by showing the difference between volume and surface conduction. We identify the G^4-FET regions of operation where conventional concepts

Manuscript received December 30, 2003; revised June 22, 2004. This work was supported by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration. The review of this brief was arranged by Editor T. Skotnicki.

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Digital Object Identifier 10.1109/TED.2004.836548