Behavioral Simulation Techniques for Substrate Noise Analysis in PLL Circuits

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Abstract- This paper presents a methodology to simulate, at the system level, the substrate noise coupling to phase locked loop (PLL) circuits in mixed signal systems. Macro-modeling for digital noise injection and propagation through the substrate are considered. Behavioral models of the PLL for noise sensing as well as intrinsic functionality are abstracted from transistor level circuit analysis results. An impulse sensitivity function (ISF) technique is proposed to characterize the substrate noise effects on the phase perturbation of the voltage controlled oscillator (VCO). Verification uses time-domain analysis with a simulator and abstracted behavioral models, all implemented in the C++ language. Compared to the traditional circuit level simulation method, this approach provides several orders-of-magnitude improvement in speed with acceptable accuracy in terms of phase noise spectra.

I. Introduction

Mixed signal, system-on-chip (SOC) implementations are of growing importance, compared to multi-chip solutions, due to their area and cost efficiencies. However, these systems also have drawbacks due to the noise coupling between digital and analog circuits through the substrate and power distribution nets. Basically, this noise consists of three main components: noise injection from the digital blocks, noise propagation through the substrate and noise coupling to the analog blocks [1]. For each of these components, different analysis and simulation results have been proposed in the literature; particularly, for the noise injection into analog circuits, transistor level simulation has traditionally been used [2] [3].

While simulation at the circuit level provides accurate results, it requires extensive computation over extended time periods, especially when performing transient analysis of complex circuits such as those involving phase locked loop (PLL) circuits. The simulation of PLLs requires transient analysis with small time-steps over long intervals in order to achieve accurate results at the circuit level. Moreover, this situation becomes worse as the center frequency of the PLL increases due to the maximum frequency limitation (1/2T). Very often, however, it is necessary to simulate the system in a coarse but fast way in order to gain initial design guidance. For example, speed is more critical than the accuracy when simulations need to be repeated in order to identify key parameters in the design. In these cases, a behavioral-level modeling technique can be a powerful option to exploit trade-offs between simulation time and accuracy. Although behavioral simulation for PLLs has been studied from many perspectives, including noise considerations [4] [5], a macro model for the substrate noise coupling has not yet been seriously addressed.

This paper will first discuss the general concepts of macro-modeling techniques for behavioral simulation in mixed signal systems. Then, a method for modeling the substrate noise coupling to PLLs at the system level using an impulse sensitivity function (ISF) will be discussed. This includes detailed considerations of the circuit-level performance issues. Finally, the efficiency of the proposed behavioral simulation methodology in analyzing substrate noise will be validated by comparing both speed and accuracy with the full circuit level simulation results.

II. Modeling Methodology for Mixed Signal Systems

While the behavioral simulation technique has the advantage of faster computational speed, it provides only coarse-grain results. In order to guarantee the accuracy as well as speed of the behavior simulations, it is critical to carefully abstract the characteristics of each block, for use at the system level model, from the circuit- or device-level analysis. For this abstraction process, three general approaches are considered:

1) If a circuit block is characterized with steady state or periodic operation, it can be modeled by simplifying the circuit or device level simulation result;
2) If the block operates over a long transient period, a mathematical behavioral model based on its temporal functionality needs to be derived over the entire simulation period;
3) If the block exhibits linear and time invariant properties, a transfer function approach can be used to create a macro model.

These proposed approaches are applied to the sub blocks of a typical mixed signal system. Macro models are thus obtained for noise injection, propagation and coupling,

respectively. The procedures for creating each aspect of substrate noise behavior model are now discussed.

A. Phase Locked Loop Circuit

In the mixed signal system considered here, a phase locked loop (PLL) circuit is a victim of substrate noise, coupling from digital noise sources. Therefore, its behavioral model should have two components: representation for its temporal functionality and a description for the substrate noise coupling. While the functional model simulates ideal PLL behavior at the system level, the noise coupling models determine and add the substrate noise effects that occur during transient analysis.

Since a core component of the PLL is the voltage controlled oscillator (VCO), the characteristic transfer curve relating output frequency to the VCO input voltage is critically important in abstracting the PLL behavior model. Hence, the VCO is simulated at the circuit level with varying input voltages; a mathematical polynomial equation is then determined by curve-fitting the data (Fig. 1). In addition, several key parameters for the PLL are specified: the amplitude of the switching current in the charge pump, the transfer function of the loop filter and the division value of the divider. The ideal temporal behavior of the PLL can then be simulated at the system level, using these equations and parameters. While most parameters can be easily determined from simple circuit-level simulations or design net-lists, the characteristic transfer curve of the VCO demands sizable computation time – 20 hours for the curve of Fig. 1.

Other than these dependencies, the actual noise coupling mechanisms to the PLL need to be identified and abstracted to the system level, using both numerical analysis and circuit level simulations. In terms of the substrate noise sensing, the constituent components of the PLL can be categorized as follows: VCO; loop filter; and other digital blocks including charge pump, PFD and divider. For each component, the circuit level simulation with periodic digital switching noise through the substrate network [3] was performed and the effects of noise were examined. Observations from the simulations show that the digital blocks do not play a significant role in the substrate noise sensing through the bulk node of transistors, mainly because in most of the circuits substrate noise is intrinsically less destructive to the digital blocks than to the very sensitive analog blocks. In contrast, the loop filter was severely impacted by substrate noise since the capacitors and resistors in the layout of the filter have direct coupling between the VCO input node and the substrate. Thus, substrate noise is strongly coupled to the PLL through the loop filter. Furthermore, the noise also affects the VCO directly: substrate noise which is injected to the bulk node of the transistors in the VCO causes a significant disturbance in observed drain currents. This current variation results in a phase shift at the output of the VCO [6].

Although these two coupling mechanisms – loop filter and VCO - are equally significant in contributing to the phase noise of the VCO, there is a basic difference in the approach needed to obtain the respective macro models. Since the subs-

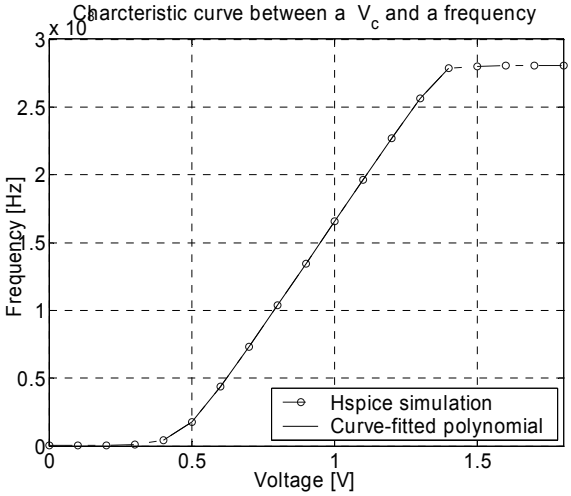

Fig. 1. Characteristic curve between the output frequency and the VCO input

rate coupling mechanism to the VCO input through the loop filter is linear and time invariant, the transfer function of the loop filter based on using a characteristic curve between the output frequency and the VCO input is sufficient for its behavioral model. However, the coupling mechanism through the bulk node is time variant as well as spatially distributed, since the operating conditions of the transistors in the VCO change with time. A different approach to model this time variant mechanism will be discussed in section III.

B. Noise Injection from the Digital Circuitry

Since the substrate noise coupling to the victim blocks cannot be guaranteed as linear and time invariant, the digital noise should be defined in the time domain, rather than in the frequency domain. In other words, transient analysis is the only way to characterize the digital noise to analyze substrate noise effects in mixed signal systems. However, as in the case of PLLs, this transient analysis is often computationally demanding; thus, a macro-modeling approach is needed for these noise injection mechanisms. Because the dominant digital noise injection process in the mixed signal systems is di/dt noise on the supply rails [7], the current noise waveforms on the supply and ground lines become a focal point in the model abstraction process. In order to abstract the current noise waveforms, two different methods are involved: 1) mathematical modeling to capture global noise patterns and 2) extraction of the basic pulse shapes from the circuit level simulation. The choice between the two methods depends upon the complexity of the structures and the switching information available for the digital blocks.

When extracting the current pulses from the circuit level simulation, the time resolution needs to be considered carefully for two reasons. First, this resolution will also be required in the system level simulation. Because the time step of the system level simulation, T, specifies the maximum frequency, 1/(2T), in the spectrum analysis, the required resolution must accurately capture the center frequency of the PLL and the frequency range of interest for the digital noise. Second, the resolution needs to be smaller than the falling and

rising times of digital switching in order to achieve a reasonable extraction; thus, the digital switching characteristics should also be considered in deciding the time resolution of the circuit level simulation.

In this work, the basic element used to generate the digital noise is a simple inverter (or a chain of them) with periodic switching. In this case, the extraction of the current pulse shape from the circuit level simulation over a period of digital switching is sufficient to abstract the digital noise. The basic pulse is then mathematically expanded into a current noise sequence using convolution of the basic pulse with an impulse train. The sequence should be sufficiently long for the transient simulation of the PLL. The above method can be applied to more complex digital circuitry as long as its current noise pattern is periodic. Moreover, even when the current pattern is not perfectly periodic, the method is still valid if the aperiodic noise components are negligible, compared to the other parts. The essential concept is to decompose the current noise pattern and the related circuit block into periodic and apeiordic parts and to validate that the above method is applicable.

If the current noise pattern cannot be identified as periodic, the extraction of temporal switching information, using appropriate hardware description languages [8], is more practical for determining the global noise pattern, rather than the mathematical modeling approach.

Finally, additional numerical adjustments must be performed on the abstracted current noise, because the behavioral simulation requires noise in a voltage format. Since the voltage noise of interest is caused by di/dt noise through the bonding pins in the package, a voltage noise pattern can be obtained by taking the derivative or by using first order differences of the current noise.

C. Noise Propagation in the Substrate

Since the substrate is generally considered as a passive network in mixed signal systems, LTI (linear and time invariant) properties with the transfer function can be exploited for its macro model, as proposed in section II. It also can be assumed to be resistive up to the orders of GHz [9]. Consequently, in this work the macro model of the substrate network uses a simple attenuation factor of the noise source. This factor depends on specific features of the substrate: the doping type of the substrate and contact distribution for the supply and ground nets, as determined by the system layout. Based on these features, resistance values between contacts are extracted from device simulation and then, the scaling factors are determined using circuit level simulation of the network.

This paper assumes that the substrate uses an epi-layer on a heavily doped bulk in which the single node approximation [2] is applicable; a resistive network structure is adopted from other studies [3].

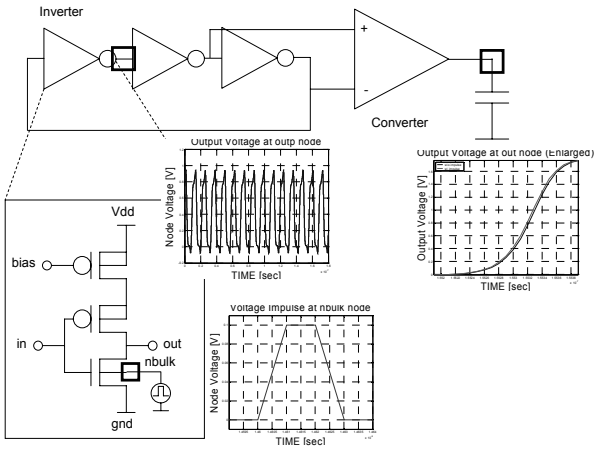

Fig. 2. Hspice set-up for the substrate noise coupling to a ring oscillator type VCO

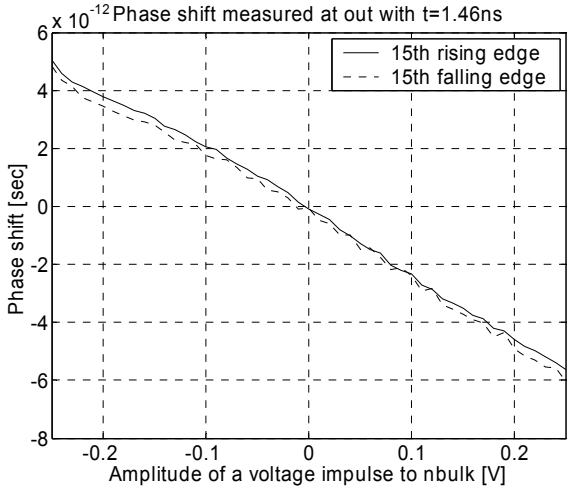

Fig. 3. Phase shifts with the amplitude of the impulse changing

III. Macro Model for the Substrate Noise Coupling Mechanism to the VCO in a Phase Locked Loop System

As explained in section II.*A*, the VCO within the PLL is the most noise sensitive block. The noise, coupled through the bulk node of transistors in the VCO causes a phase shift at the output of the VCO. This coupling mechanism is linear and time variant: as the amplitude of substrate noise increases, the amount of this phase shift increases linearly; and the phase shift is also dependent on the moment when the noise is coupled. Fig. 2 shows the Hspice simulation set-up for substrate noise and phase shift analysis. A voltage impulse is applied to the bulk node of an NMOS in a ring oscillator type VCO and the steady state phase shift at the output of the converter is measured. Fig. 3 shows the correlation between the amplitude of the impulse and the corresponding phase shifts. The results demonstrate linearity within a reasonable range of the noise amplitude; the typical amplitude of substrate noise is observed to be around 100-200mV [10].

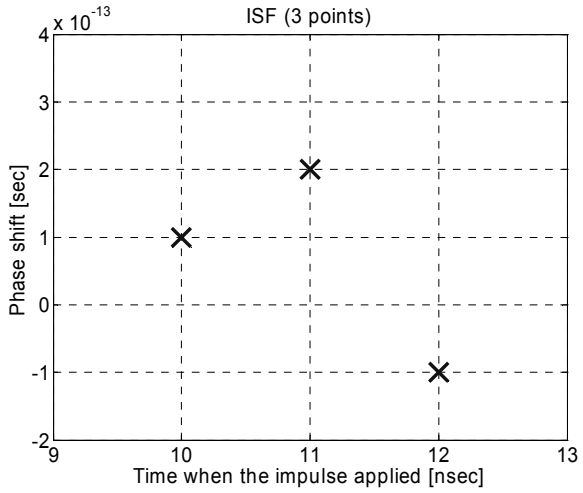

Fig. 4. Phase Shifts with the applied time of the impulse changing

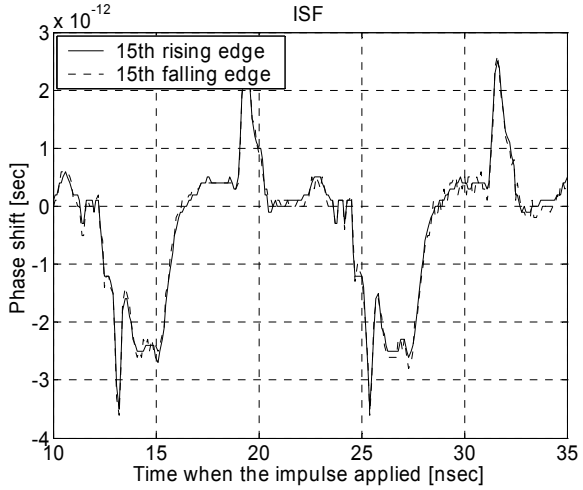

Fig. 5. ISF data, measured two different edges

The time variance is also shown in Fig. 4. With a fixed amplitude of 100mV, the impulse is applied at three different moments, and the resulting phase shifts are observed to have different values.

This linear and time variant relationship between substrate noise and phase shift can be characterized using the impulse sensitivity function (ISF), first proposed by Hajimiri et al. [6]. The ISF can be accurately determined by circuit level simulation, using the set-up in Fig. 2. Data for the entire function are shown in Fig. 5, which is basically an expansion of Fig. 4 over the period of the VCO. That is, the simulation in Fig. 2 is repeated, applying a voltage impulse at every moment over the period and the observed phase shifts are displayed in x-axis of the applied time and y-axis of phase shifts. In order to ensure the steady state, phase shifts are measured at two different edges of the converter output waveform. With the Hspice, this extraction process took approximately 5 hours.

Fig. 5 illustrates two main characteristics of the ISF. First, the function is periodic, because the operating conditions of the transistors in the VCO are also periodic. As a result, the ISF shares the same period with the VCO. Second, the ISF can be decomposed into symmetric and asymmetric parts in terms of polarity, as clearly displayed again in Fig. 6. In fact, these components are attributed to two fundamental substrate noise coupling mechanisms of MOS devices-- the body effect and capacitive coupling [11].

The body effect for MOS devices disturbs the drain current which yields a phase shift. These two connected variables are characterized by the parameter, g_{mb} and another type of ISF which depends on the current impulse, ISF_i [6], respectively. Consequently, the multiplication of both parameters should correspond to the sensitivity component related to the body effect in the ISF of Fig. 5. Fig. 7 compares the product of g_{mb} and ISF_i with the ISF and demonstrates that the asymmetric part of the ISF is contributed by the body effect. On the other hand, the symmetric part should be attributed to capacitive coupling. This part is closely related

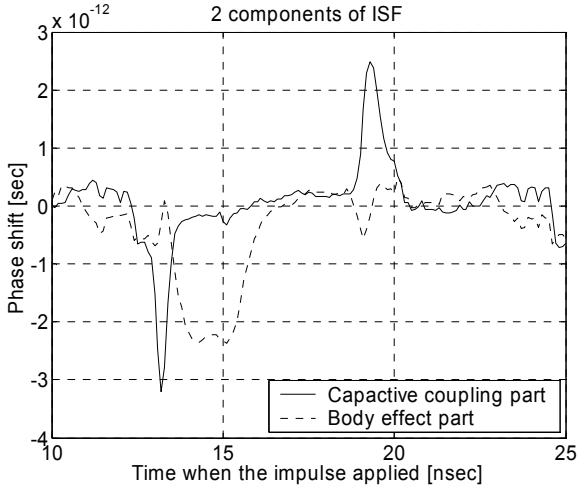

Fig. 6. Two components of the ISF

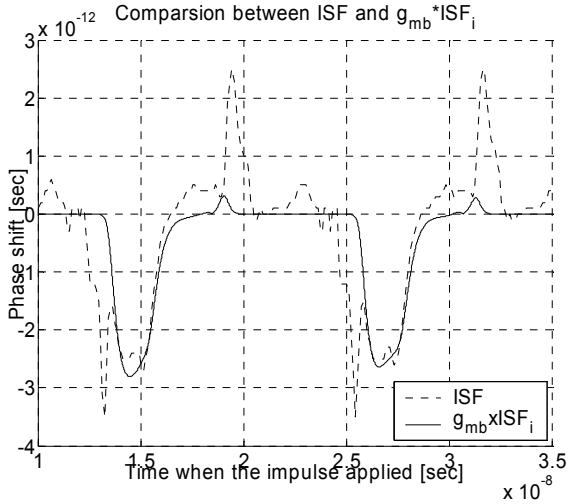

Fig. 7. Comparison between the ISF and gmb×ISFi

to the switching behavior of the transistors; thus, its greatest impact is concentrated around the transition edges of switching activities because the coupling capacitance increases at these points due to the Miller effect. Moreover, this part is symmetric since the capacitive coupling environments are opposite at the rising and falling edges of the transitions.

Once the ISF is determined, the phase shift or phase noise is calculated by:

$$\Delta\Phi(t) = \int_0^t v_{substrate}(\tau) \times h_{ISF}(\tau)\, d\tau$$

Since the system level simulation operates on discrete time data, the integration needs to be replaced by a summation in the implementation. Fig. 8 provides the system level block diagram of the VCO.

IV. System Level Simulation Process for the PLL

Once the macro models are determined using the techniques proposed in sections II and III, the substrate noise effects for the entire mixed signal system can be simulated at the behavior level. Since the digital noise injection and propagation models can be determined as a pre-process step, the behavioral simulation can mainly focus the noise coupling to the victim PLL. This simulation process for the PLL includes two main components: the main transient simulation of the PLL behavior in C++; and the numerical data analysis, using MatLab. The C++ simulation uses pre-defined libraries available at http://www-mtl.mit.edu/~perrott [4], which provide macro models for each block in the PLL: PFD, charge pump, loop filter, VCO and divider. The parameters, extracted from circuit level simulations, specify these models; the assembled models in a closed loop are simulated in the time domain. This simulation is usually effective with the phase-locked, steady state behavior of the PLL and not quite accurate for the initial transient state. The transistor level design of the PLL is provided by Barcelona Design Automation (http://www.barcelonadesign.com/) and the block diagram of the entire PLL structure is presented in Fig. 9.

The C++ simulation is based on discrete event modeling and thus requires careful choice of the time step. The selected values should be able to support the center frequency of the PLL and the observed spectral range for noise, as explained in section II.*B*. The number of sampling points, N, is another important factor in the simulation. That is, because it defines the frequency resolution, 1/(TN), the larger number of sampling points, the better the resolution. Even so, since the number of points is directly related with the simulation time, it cannot be increased arbitrarily.

The data analysis of the system level simulation results is another important issue. While the noise injection is easy to handle in the time domain, the noise effects on the PLL output are more easily observed in the frequency domain, thereby requiring a high resolution for both the time and frequency domains. Furthermore, since the analysis method uses the fast Fourier transform (FFT) algorithm, several issues should be considered to avoid aliasing of the spectrum with the given frequency resolution. First, the sampling frequency of the C++ simulation should be an integer multiple of the reference frequency of the PLL and another sampling frequency in MatLab (or other data analysis tool) unless it is much greater than those frequencies. Second, the basic clock frequency of the digital noise should be carefully chosen so that the frequency peak caused by the noise is not to be confused with other peaks caused by aliasing. Finally, if the circuit level simulation cannot support the same sampling frequency as in the C++ code, interpolation can be used for abstracting the data. When considering the above issues, comparing the data with the circuit level simulation results can be helpful to ensure that the behavioral simulation set-up has sufficient resolution and avoids aliasing in the frequency range of interest.

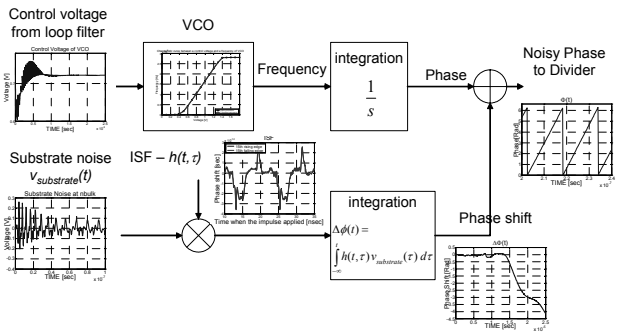

Fig. 8. System level block diagram of the VCO

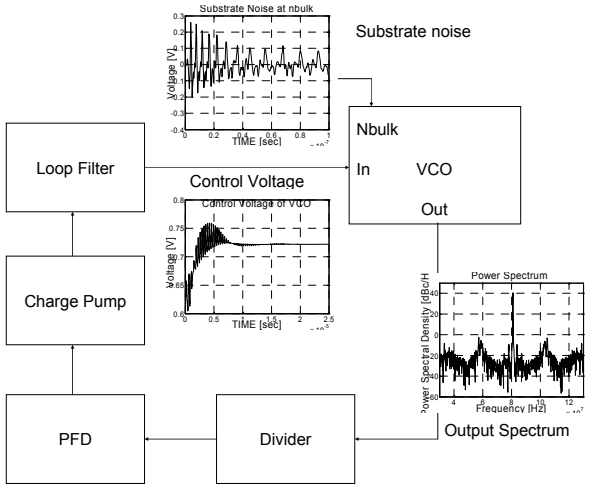

Fig. 9. Block diagram of the PLL at the system level

V. Simulation Results and Validation of the Behavioral Simulation Efficiency

Based on the transistor level design of the mixed signal system, which consists of a digital noise emulator (DNE), a substrate network [3] and a PLL, the Hspice simulation was performed to validate the efficiency of the behavior level simulation. The CMOS technology of the simulation is TSMC .18μm process. In order to focus on the behavioral simulation part of the PLL for the verification, the digital noise pattern at the system level was simply extracted from the Hspice simulation. Moreover, the substrate noise is assumed to be coupled to the bulk node of only one NMOS so that a single ISF can be clearly examined. In more general cases, substrate noise is coupled to the bulk node of all the transistors in the VCO as common mode noise. Hence, the coupling mechanism can be modeled as the superposition of ISFs.

The DNE takes a clock input and operates several blocks in different branches: a buffer chain, a pseudo random bit sequence generator and a divider, each of which can be activated separately so that the DNE can generate various digital noise patterns.

Table 1 shows the basic simulation conditions. The time step for the C++ simulation is determined from the effective width of the pulse which is used to extract the ISF. The larger time step is chosen with the Hspice simulation in order to maintain reasonable simulation time.

Fig.'s 10 and 11 compare the PLL output spectra from Hspice and the C++-based simulator results for different DNE set-ups. As can be seen in Fig. 10, in which the random bit generator is activated, there is a reasonable correlation between the two sets of simulation results. In particular, the behavior level simulator can accurately estimate the phase noise pattern near the center frequency. When the divider-by-16 block is activated in the DNE, the low frequency component of substrate noise increases and the system level simulation can predict this effect, as shown in Fig. 11. The discrepancies at the peaks which are 3MHz apart from the center frequency are caused by the difference of the control voltages to the VCO between two simulations. In the PLL, 3MHz reference input is coupled to the VCO input and two simulation methods showed different degrees of the coupling. The resolution of this discrepancy will be one of our future works.

Although small discrepancies are observed between two spectra, the improvement in computation time is considerable. While the Hspice simulation demands more than 37 hours on the Ultra Sparc 2 machine, the C++ base simulation results take only 2 minutes. These results show that the system level simulation provides sufficient information to predict the substrate noise effect approximately 1000 times faster than that for the circuit level simulation.

TABLE I
Simulation Conditions

Conditions	Hspice	C++
Time Step	200ps	20ps
Time Duration[1]	12.5μs	10μs

[1] in phase-locked, steady state

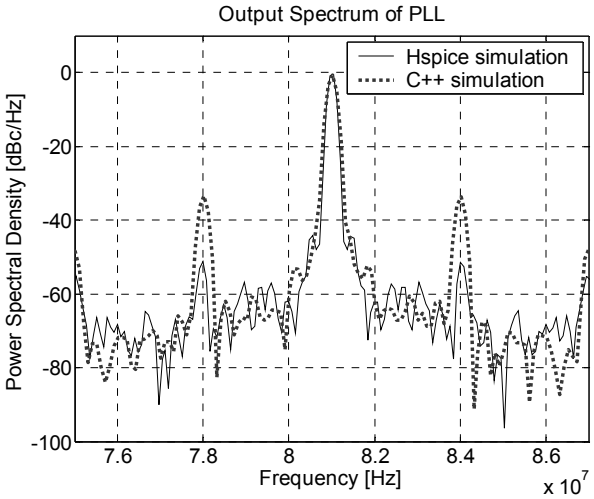

Fig. 10. Comparison of output spectra when the pseudo random bit sequence generator activated

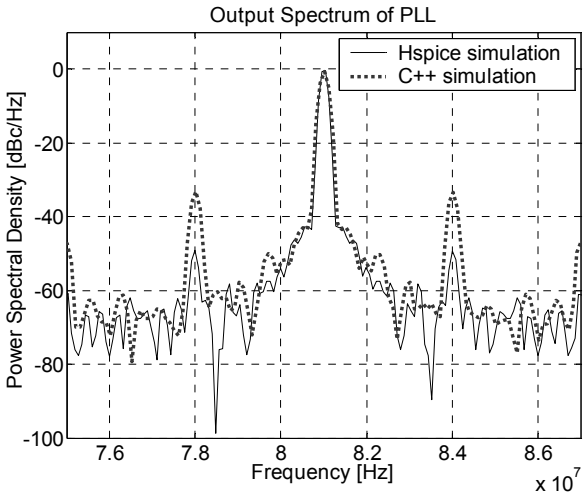

Fig. 11. Comparison of output spectra when the divider-by-16 activated

VI. Conclusions and Future Work

We have considered a system level behavioral simulation methodology to analyze substrate noise issues in mixed signal systems and have discussed general issues of macro-modeling for noise injection, propagation and coupling. We proposed a noise coupling mechanism model for the VCO, using the concept of an impulse sensitivity function (ISF) for that block. Finally, a comparison between Hspice and C++-based simulator results validates the efficiency of the behavior level simulations. More detailed analysis and applications of the ISF can be extracted. In addition, models for the noise coupling mechanisms of components other than the VCO in a PLL system should be developed to achieve more comprehensive behavior models for noise coupling.

Acknowledgement

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