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24 Efficient Techniques for Reducing Substrate Model Complexity in Mixed-Signal IC's
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Efficient Techniques for Reducing Complexity of Substrate Models in Mixed-Signal IC's

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Abstract- This paper presents a hybrid modeling scheme for reducing complexity in creating substrate models. Mathematical estimation reveals the difficulty of grid connection and full connection structures when dealing with large number of contacts. Device simulation shows the relative significance of far-field and near-field effects. The proposed hybrid model scheme decomposes large scale problems into smaller scale, near-field, far-field, and local fully-connected model problems to reduce the overall substrate modeling complexity. The model is applied to a heuristic prototype example and is discussed in the context of a real mixed-signal design example. The model is shown to be useful in reducing the complexity for typical substrate models.

I. Introduction

Driven by the increased industry interest in system-on-a-chip (SoC), there has been substantial research effort to address the substrate noise coupling problem. With smaller signal headroom and more stringent specifications in today's analog and RF circuitry, sensitive parts of the circuitry become more and more vulnerable to noise from digital circuitry, including package parasitics. Efficient modeling and simulation of substrate noise coupling is thus a challenging and critical issue in mixed-signal IC designs.

There have been several numerical techniques and equivalent circuit modeling approaches for considering substrate noise coupling. Most numerical techniques employ fine-grid meshes and therefore are computationally intensive [1]-[6]. This becomes impractical when dealing with real chip design where the number of contacts can easily be greater than several thousand. Some macro modeling methods employ the full connection port-to-port parameters [7]-[9]. This approach faces geometrically increasing complexity on the full chip level simulation.

In this paper, a novel modeling strategy for combining near-field, far-field, and local fully-connected models is proposed to reduce the substrate modeling complexity, while still allowing practical simulation of substrate coupling in mixed-signal IC designs.

First, the mathematical estimation of the complexity of different substrate models is considered. 3D device-level simulation shows the near-field and far-field effects. A hybrid model is proposed. The modeling approach is then applied to a canonical example. The resulting model is compared with full chip, 3D device-level simulation results. The potential application in a real mixed-signal design is then discussed. Finally, conclusions are presented.

II. Substrate Model Complexity Calcultion

From a modeling point of view, although the substrate is neither homogeneous nor isotropic, the gradient of doping concentration can only be observed in the direction normal to the chip surface. Thus the substrate can be always treated as a layered structure, as shown in Fig. 1(a). Within a layer, grid connection model shown in Fig. 1(b) and full connection model shown in Fig. 1(c) are the two most widely used types of the substrate models [3][7][9]. Since the model complexity determines the feasibility of the implementation into CAD tools, it is very important to keep these numbers finite. For a substrate with dimensions $L\times W\times H$ (length, width, and height, respectively) the model complexity can be calculated as follows.

Given the total number of substrate contacts to the chip surface is $N = (n+1)^2$, there are I segments between two specific nodes, and J segments into the substrate. The complexity for grid connection, O_{grid}, and for full connection, O_{full}, can be approximately expressed as Eq. (1) and Eq. (2), respectively:

$$O_{grid} = J\cdot(I\cdot n)^2 = O(J)\cdot O(I^2)\cdot O(N) \quad (1)$$

$$O_{full} = J\cdot I\cdot C(N,2) = O(J)\cdot O(I)\cdot O(N^2) \quad (2)$$

At first glance, since I and J are much smaller than N in most cases, the grid connection option might be preferred because of its lower complexity. However, if S-parameters between two distant nodes are of primary interest to the designers, the full connection model would be a better choice. The conductance matrix obtained from the full connection model

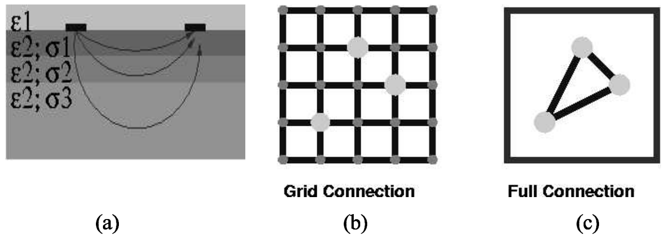


Fig. 1. (a) Layered substrate structure (b) Grid connection and (c) Full connection

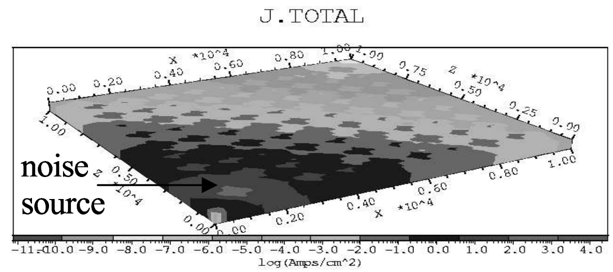


Fig. 2. 3D DAVINCI simulation shows that the distant contacts are less likely to be affected.

can be easily converted to *S*-parameters by using the equations in [10]. On the contrary, it is not as easy for the grid connection model since there is no direct connection between those nodes in such scheme.

From the above derivation, it is clear that the number of substrate contacts is one of the limiting factors for the full connection model.

In the local, fully-connected model, only the contacts located within the assigned distance, *d*, are fully connected. In other words, for any two nodes with a distance greater than *d*, the circuit elements connected between them are eliminated. This model preserves direct access to *S*-parameters between nearby nodes and reduces the number of connections. The complexity for this new model, O_{loc}, is shown in Eq. (3):

$$\begin{aligned} O_{loc} &= 0.5 \cdot J \cdot I \cdot C(N,1) \cdot C(N \cdot d^2/(L \cdot W),1) \\ &= O(J) \cdot O(I) \cdot O(N^2 \cdot d^2/(L \cdot W)) \end{aligned} \quad (3)$$

Fig. 2 shows the voltage potential contours obtained by 3D DAVINCI device-level simulation. The structure has dimensions of 5mm × 5mm × 250μm with 81 substrate contacts uniformly distributed on the chip surface. The voltage type noise is in-jected into the substrate from the contact on the lower corner, as indicated in Fig. 2. The plot of current density distribution illustrates that distant contacts are less likely to interact with the injection node. It further justifies the local, fully-connected model.

The complexity of different models is compared in Fig. 3. As shown in that figure, the complexity of pure grid connection is lower than the complexity of the pure full connection. They both have high complexity when the number of contacts is in the order of 10^2. It can also be seen that for the full connection structure, the number of connections can be greatly reduced by properly choosing the coverage factor, which is defined as:

$$\alpha = d^2/(L \times W) \quad (4)$$

For example, the complexity can be reduced by a factor of 10^2 with the coverage factor of 0.01. It indicates that a local, fully-connected model is suitable in preserving the advantage of full connection with much lower complexity.

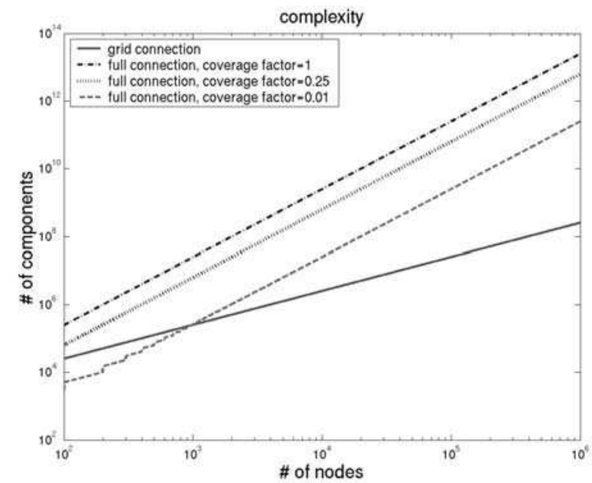


Fig. 3. Complexity calculation: 10 segments down to the substrate, dash-dot: full connection, dot: local full connection with coverage factor 0.25, dash: local full connection with coverage factor 0.01, solid: grid connection.

III. HYBRID MODEL

Both the grid connection model and the full connection model are able to address small scale problems efficiently, where the number of contacts is less than the order of 10^2. However, in practical mixed-signal IC designs there are typically thousands of contacts. Using either the grid connection or full connection models leads to a huge number of components and this may exceed the maximum grid number that is feasible for practical simulation. Therefore, neither the conforming grid meshing scheme nor the full connection can be efficient in practice.

In substrate noise coupling analysis and modeling, the most critical thing is the coupling path between the contacts or IP blocks where the digital noise is generated and the contacts or IP blocks where the most sensitive circuitry exists. For both the noise source end and the noise sensor end, fine resolution is very important in order to characterize near-field effects. Between the noise source and the noise sensor, it is typically the far-field effects that dominate. The contacts other than those located in the direct coupling path have relatively less influence on the coupling between the noise aggressor and the noise victim. Detailed 3D device simulation reveals that distant contacts are less likely to be affected, as shown in Fig. 2. Similar idea based on far-away and neighboring coupling has been investigated in the context of on-chip interconnect [11].

A hybrid modeling approach is proposed here based on the above physical interpretation. Fig. 4 illustrates the general model topology. First, a coarse mesh is used on the given circuit layout. The contacts enclosed by a coarse mesh can be treated as local, near-field, contacts. The contacts surrounding the noise source are modeled by a near-field model (*NFM*). The near-field contacts close to the noise sensitive circuit are modeled by a local, fully-connected model (*LFCM*). The direct, long range, coupling path between the aggressor and the victim is modeled by a far-field model (*FFM*). A representative NFM is constructed using a parallel connection of resistances, which models the noise current sinked by the contacts around the noise injection contact. The LFCM can be a resistance network consisting of the resistances between any two contacts. The FFM can be as simple as a single resistance. It should be noted, however, that the FFM can also be a RC or even RLC circuit for very high frequency applications where delay effects become significant. The topography consisting of NFM, FFM and LFCM is generally valid while their specific forms for each case can vary, depending on the modeling requirements.

The big advantage of the proposed hybrid model is that it can greatly reduce the model complexity compared to either the pure grid or full connection options. Once the digital noise signature is given or pre-determined, the portion of the noise propagating to the far end noise sensor can be computed using the NFM, which essentially counts how much noise is extracted by the nearby contacts, e.g., guard bands. Since the victim region is modeled using a fully-connected model only locally, as its name LFCM suggests, the complexity of the LFCM is typically low. The LFCM should be used to model regions near the noise victim. Thus the contact location pattern should remain as a static structure for extraction of the LFCM, in order to achieve the required locally fine resolution. On the contrary, for the other non-critical regions it is not necessary to use the LFCM. It is desirable to use the contact aggregation algorithm in such regions. Meanwhile, the FFM can be determined by measuring or simulating the port-to-port *z*- or *y*-parameters between the aggressor and the center of the victim region, modeled using the LFCM or the locally aggregated and weighted contact regions. The FFM thereby embeds most of the spatially dependence information.

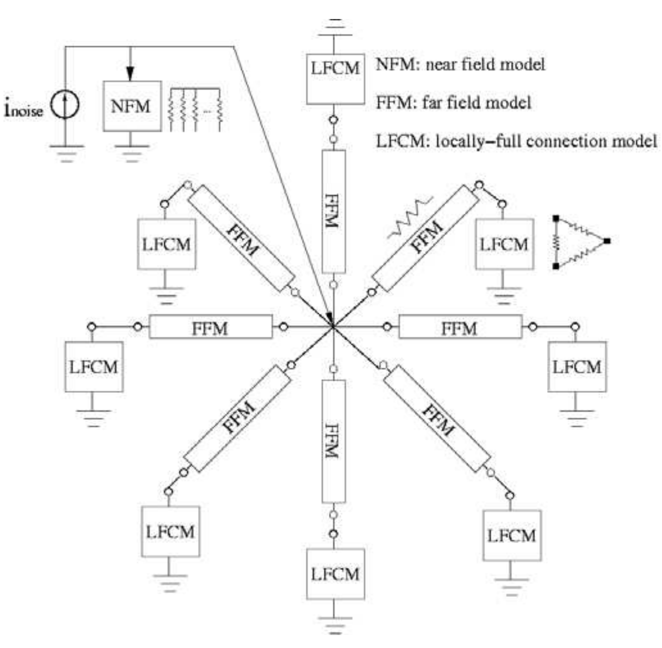


Fig. 4. Diagram of the hybrid modeling scheme.

IV. Application Examples

A. A Heuristic Star-Pattern Layout

Fig. 5 shows a heuristic star-pattern test layout. The dimensions are 100 μm by 100 μm by 250 μm. All the labeled contacts are p+ contacts with doping concentration $Na=1\times10^{20}$ cm^{-3}, depth 0.2 μm and size 10 μm by 10 μm. The substrate is a lightly doped bulk silicon with doping concentration $Na=4.0\times10^{16}$ cm^{-3}. The contact labeled NS is assumed to be the noise source and the one labeled A4 is assumed to be the noise sensor. The remaining contacts represent the influence from other circuit blocks or IP blocks, or noise isolation features such as guard bands.

First, a uniform coarse mesh is used to differentiate the near-field and far-field regions. Considering the entire layout dimensions and the contact feature sizes, a meshing scheme with grid to grid spacing of 30 μm is reasonable for this specific example. As a result, it can be seen that the contacts A1 to H1 are on the same mesh spacing as the noise source NS and thus they need to be modeled using the near-field model, i.e., NFM. Meanwhile, A2 and A3 are on the same mesh as the noise sensor A4 and thus they should not be aggregated in order to preserve the locally fine resolution, which is critical to the accurate prediction of how much noise that A4 can sense. Thus these blocks need to be modeled using the local, fully-connected model, i.e., LFCM. For other contacts which are neither within the NS near-field region nor the A4 near-field region, it is reasonable to simply aggregate their effects as weighted contact regions by using the following formula:

$$A_{aggregated} = \sum_{\text{all local contacts}} A_i \tag{5}$$

where A denotes the area of contact. The resulting new weighted contacts can be placed at the center of the local regions. Then the far field model, i.e., FFM, can be developed by examining the port parameters between the noise source and the new weighted contact region. The FFM essentially carries the long range geometrical information between the

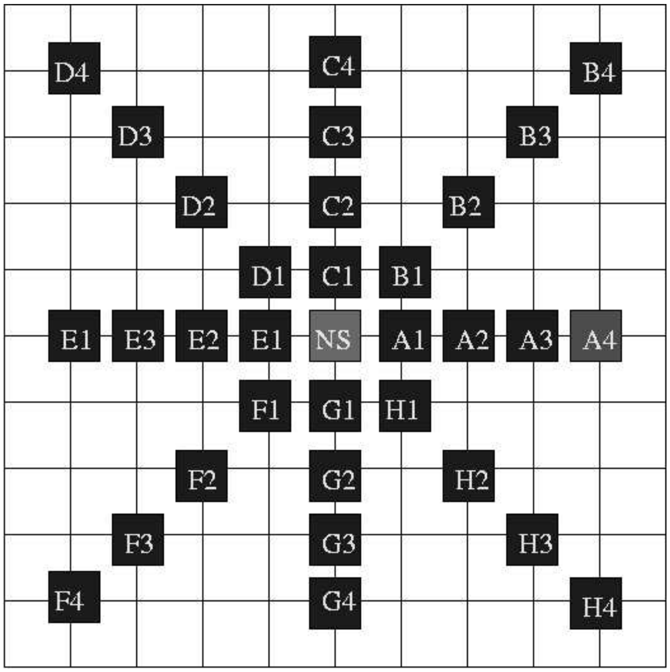


Fig. 5. A star-pattern test layout. The contact NS is the noise source and the contact A4 is the noise victim.

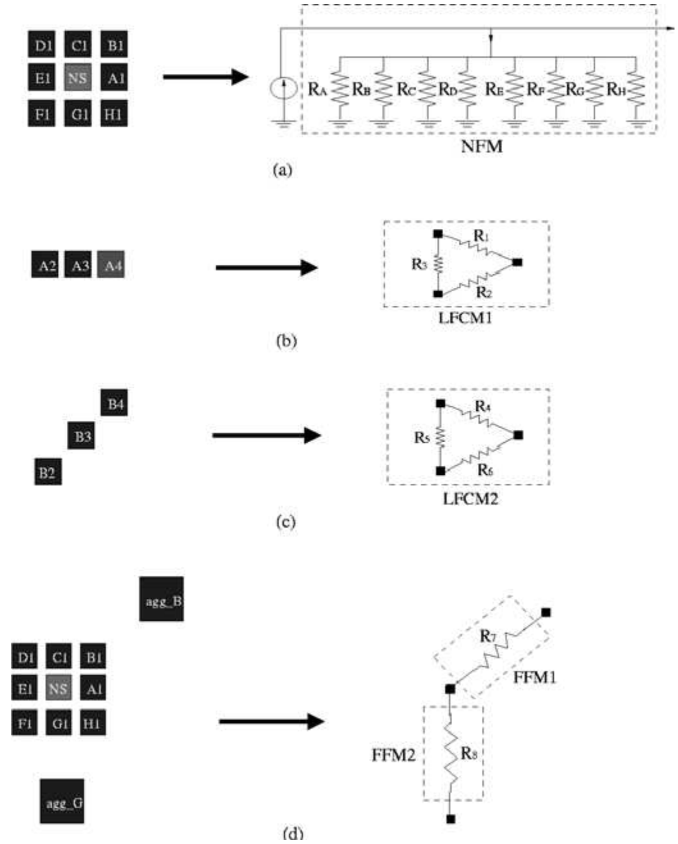


Fig. 6. Model development of (a)NFM, (b)(c)LCFM and (d) FFM for the star-pattern layout example.

noise aggressor and victim and thus should be distance dependent.

Fig. 6 shows the model development for the NFM, LCFM and FFM used in this example. Fig. 6(a) shows the NFM that characterizes the near-field contact influence on the noise injection from NS. In the NFM, each branch resistance in the parallel connection characterizes the noise sinking capability of one nearby contact. A significant portion of the noise can be absorbed by the local near field contacts. The rest of current noise becomes the noise propagating over the entire chip through substrate coupling effects on the other contacts. Fig. 6(b) and (c) show respectively the locally fine models for the horizontally (or vertically) oriented contact pattern and the 45 degree tilted contact pattern, namely, LFCM1 and LFCM2. Note that in this specific example, only two LFCM models need to be developed. Basically, the LFCM is used to model the local geometry dependent noise sensing. Fig. 6(d) shows the FFM between the noise source region and the distant aggregated contacts. Again, only two FFMs need to be developed. Table I lists the extracted resistance values. As expected the resistances in NFM are small and the resistances in FFM are large.

Fig. 7 shows the complete circuit model generated by fitting the NFM, LFCM and FFM discussed above into the general hybrid model topology shown in Fig. 4. The model is compared with rigorous 3D device simulation results, as shown in Fig. 8. The comparison is summarized in Table II. The model gives less than 2.2% error when the complete circuit shown in Fig. 7 is used. Since only the region that includes the A4 contact is critical, it should not incur much lose in accuracy due to dropping (grounding) the LFCMs of the other regions. This can be done by grounding all the other near-field block models with cross marks labeled in Fig. 7. The resulting further simplified model in fact gives 3.9% relative error.

It should be pointed out that all these demonstration models have been generated using scaled layout configurations and thus the model development efficiency is much higher than that of full connection or grid connection methods applied on the original entire layout configuration. Another advantage of the hybrid modeling approach is that it provides better design insight by decomposing the entire model into NFM, LFCM and FFM. For example, in the mixed-signal design utilizing IP libraries, one has little or no freedom in changing the circuit inside an IP block and therefore the NFM and LFCM are more likely to be fixed and can be predetermined and stored as part of each IP library. Normally the design freedom, and possibly the only degree of freedom, lies in the adjustment of the relative spatial placement, orientation, etc., between the IP blocks. This can be adequately modeled by only reconstructing FFM without altering NFM and LFCM, which are usually re-usable.

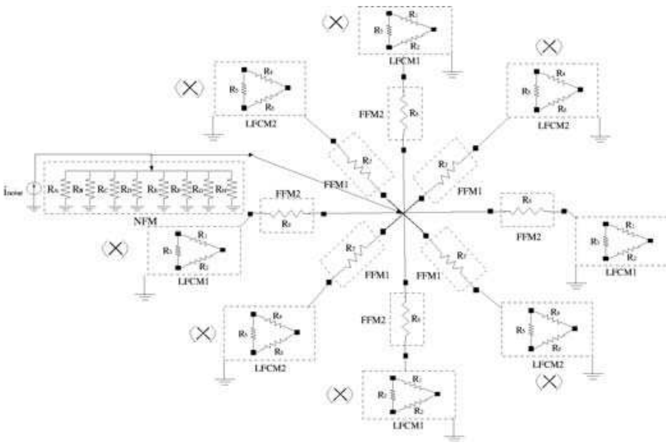


Fig. 7. Circuit modeling of the star pattern example. The LFCMs with cross marks may be dropped (grounded) without conceivable loss of accuracy for the coupling between the noise aggressor and the victim pair.

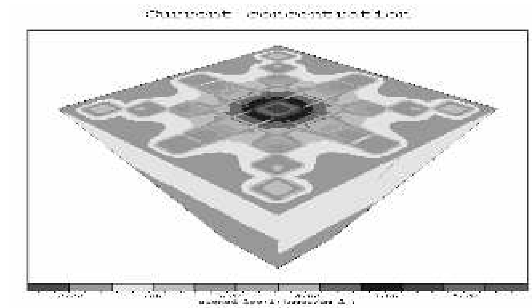


Fig. 8. 3D device simulation result of the star pattern example showing the current density distribution

TABLE I
Extracted circuit elements. All values are in Ω

R_A	R_B	R_C	R_D	R_E	R_F	R_G	R_H
116.5	322.5	116.5	322.5	116.5	322.5	116.5	322.5
R_1	R_2	R_3	R_4	R_5	R_6	R_7	R_8
62.6	206.3	62.6	88.9	376.4	88.9	1.79K	1.20K

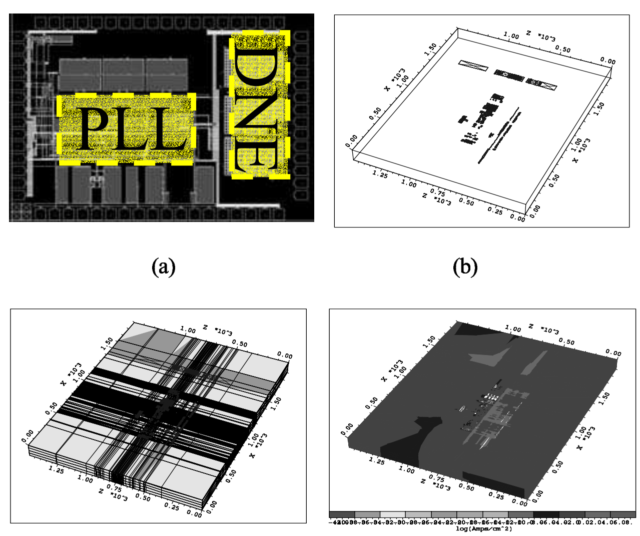
TABLE II
The comparison between hybrid model and 3D device simulation. Noise current injected at NS is 46.88 mA. (1) Complete model in Fig.3. (2) LFCM with cross mark in Fig. 3 dropped (grounded)

	(1)		(2)	
	Current noise sensed by A4	Relative error	Current noise sensed by A4	Relative error
3D device simulation	49.5 μA	2.2%	49.5 μA	3.9%
Hybrid model	48.4 μA		47.6 μA	

It is also worth mentioning that the hybrid model shown in Fig. 4 is a general diagram formulation of the scheme in decomposing large scale problem into small and hierarchical near-field and far-field model problems. The NFM, FFM and LFCM can be redefined in terms of other specific forms. It is desirable to have the NFM, FFM and LFCM with minimum coupling, in other words, decoupled as much as possible so that each of them can be independently developed. Depending on the specific application and the layout configuration, alternative forms for the NFM, FFM can also be developed. In the heuristic example discussed above, the resistance-only network is sufficient for low to medium high frequency application. However, if the frequency dependent behavior of substrate noise coupling is important, e.g., high frequency applications using a heavily doped substrate with a lightly doped epitaxial layer process, different equivalent circuit models can be adopted for the FFM rather than simple resistance structures [12].

B. Potential Application in PLL and Digital Noise Emulator

The hybrid model can be applied to real design examples. Fig. 9(a) shows the layout of a mixed-signal test chip, which mainly includes a 400MHz PLL and a Digital Noise Emulator (DNE). The DNE can emulate digital noise signatures and the noise coupling through the substrate to affect the sensitive PLL. A simplified contact configuration is shown in Fig. 9(b), where the largest digital noise sources as well as more than 100 contacts in the PLL are identified, including the major



(a) (b)

(c) (d)

Fig. 9. (a) Layout of 400MHz PLL and digital noise emulator. (b) Simplified layout location with 145 main contacts. (c) 3D conforming meshing results in $70 \times 140 \times 50 \sim 10^5$. (d) Current noise distribution from device simulation

sensitive nodes and guard rings. Using the conventional grid connection, a 3D conforming mesh can be used as shown in Fig. 9(c). This scheme results in total grid of about 10^5, which is approaching the practical upper limit for standard configuration of 3D device simulators such as DAVINCI. Fig. 9(d) shows the noise distribution from the device simulation.

Although this test design can barely be analyzed at the full chip device-level simulation, even when examining a simplified version, it is obvious that it rapidly becomes unmanageable as the number of contacts continues to increase. The proposed hybrid model can be useful in evaluating accuracy-complexity tradeoff so that efficient simulation can be performed in this example. The digital noise injection part of the DNE can be modeled using NFM. The most sensitive nodes of the PLL along with the guard rings can be modeled using LFCM. Finally, the FFM bridges the NFM and LFCM regions. Further benchmarking for this design example is still in progress.

V. Conclusions

Efficient techniques employing a hybrid modeling approach for reducing complexity of substrate models has been developed. Theoretical estimations of complexity of grid connection and full connection models reveal the geometrically increasing complexity that limits conventional methods. Both mathematical estimations and device simulations justify the feasibility of combining NFM, FFM and LFCM to reduce the overall model complexity. The proposed hybrid model has been applied to a star-pattern heuristic layout example. The modeling results are shown to agree with detailed 3D device simulation with acceptable errors in the range of only several percent. The model complexity is greatly reduced compared with the grid mesh scheme. A real mixed-signal test chip design using a PLL and digital noise emulator is discussed with potential application of the proposed model. The model should be useful in efficient simulation of substrate noise coupling in mixed-signal design.

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