Analysis and Design of Distributed ESD Protection Circuits for High-Speed Mixed-Signal and RF ICs

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***Abstract*—Electrostatic discharge (ESD) protection devices can have an adverse effect on the performance of high-speed mixed-signal and RF circuits. This paper presents quantitative methodologies to analyze the performance degradation of these circuits due to ESD protection. A detailed s-parameter-based analysis of these high-frequency systems illustrates the utility of the *distributed* ESD protection scheme and the impact of the parasitics associated with the protection devices. It is shown that a four-stage distributed ESD protection can be beneficial for frequencies up to 10 GHz. In addition, two generalized design optimization methodologies incorporating coplanar waveguides are developed for the distributed structure to achieve a better impedance match over a broad frequency range (0–10 GHz). By using this optimized design, an ESD device with a parasitic capacitance of 200 fF attenuates the RF signal power by only 0.27 dB at 10 GHz. Furthermore, termination schemes are proposed to allow this analysis to be applicable to high-speed digital and mixed-signal systems.**

***Index Terms*—Broadband matching, coplanar waveguides, distributed circuits, electrostatic discharge, high-speed mixed-signal circuits, RF ICs, s-parameters, transmission lines.**

I. Introduction

ELECTROSTATIC discharge (ESD) is one of the most serious concerns in IC manufacturing. In fact, it is known to be the most common cause of all IC failures [1]. ESD is the transient discharge of static charge arising due to human handling or contact with machines. The discharge typically occurs in a very short duration on the order of 10 ns to 100 ns, with currents ranging from 1 A to 10 A. Traditionally, protection circuits are designed and employed near the I/O pins to alleviate the impact of ESD events and to improve manufacturing yields. However, as the demand for wireless (RF) and high-speed mixed-signal systems continues to increase rapidly, providing sufficient ESD protection for these systems poses a major design and reliability challenge. This is due to the fact that in applying ESD protection to these systems, the protection system must be transparent—the protection circuit must not affect the signal under normal operating conditions [2], [3]. The on-chip protection circuit is placed between the signal pin and the core circuit, as shown in Fig. 1. The protection circuit may be composed of various devices, such as diodes, transistors, or silicon controlled rectifiers (SCRs), but in all cases, these devices shunt ESD current coming from the signal pin to the power/ground supply rails and away from the core circuit [1]. However, under normal operating conditions, these protection devices present capacitances and resistances to the signal path, and at sufficiently high frequencies, the capacitances look like short circuits to ground. Thus a poorly designed protection system can generate impedance mismatches, causing reflections of signals, corruption of signal integrity, and inefficient power transfer between the signal pin and the core circuit. In addition to these problems, both the incident and the reflected signals can interfere with signals on adjacent wires through crosstalk. Also, while the operating frequency continues to rise, the size of the protection circuits and their associated capacitances are not decreasing as rapidly, resulting in increasingly inefficient power transfer. While narrowband RF operation with ESD protection is feasible by use of simple matching networks to tune out the ESD parasitic capacitance, broadband RF system protection poses a greater challenge [4], [5]. The simple approach of minimizing capacitance while maintaining high protection levels is becoming increasingly infeasible as the operating frequency rises beyond a few GHz [6]; alternate protection schemes such as the distributed transmission line ESD protection system may be necessary [7], [8]. Recent work has focused on comparison of ESD protection strategies for RF applications at 2 GHz [9]. However there is little published information that provides performance analysis of RF circuits with various ESD protection design options, particularly of the distributed protection scheme, which is attractive for operations in the multi-GHz regime. In this paper, we introduce two design methodologies to quantify the impact of the parasitic capacitance and resistance associated with various distributed ESD protection circuit designs and to optimize the number and

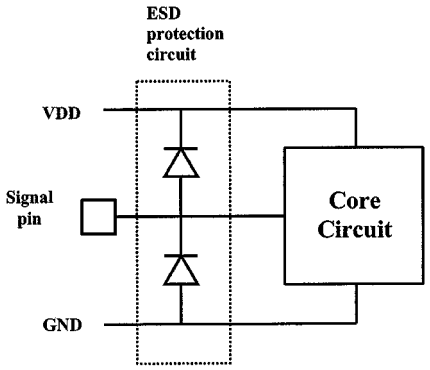

Fig. 1. A simple ESD protection system example. The diodes shunt excess current applied to the signal pin toward VDD or GND to protect the core circuit.

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length of coplanar waveguides (CPW) (used as transmission lines [10]) separating the distributed ESD elements [11], [12]. Also, it is demonstrated that a four-stage distributed ESD protection with coplanar waveguides can be employed to provide excellent RF performance for frequencies as high as 10 GHz.

II. Distributed ESD Protection System

As the operation frequency of systems rise, the parasitics associated with ESD protection systems become more significant in limiting bandwidth and power transfer. One method of minimizing the effects of these parasitics is to utilize a distributed protection scheme. A distributed ESD protection system is a modification of the distributed amplifier proposed by Ginzton [13], where ESD protection devices replace the amplifier elements. As proposed in [8], and as shown in Fig. 4(c) and 4(d), by incorporating the parasitic capacitance of the device into a discrete transmission line structure, the loading of the system by the ESD devices may be prevented.

For a constant total capacitance C, increasing the number of sections of the artificial transmission line increases the bandwidth of the transmission line. In [14], the iterative structure shown in Fig. 2 is analyzed. In the π-section shown in Fig. 2(a), the capacitance C models the ESD protection device. For the input impedance Z_i to equal Z_o, which is the load impedance of the system and also the characteristic impedance of the transmission line, the inductance L must be chosen as shown in (1), where ω_o is the operating frequency

$$L = \frac{4Z_o^2 C}{4 + (\omega_o Z_o C)^2}. \tag{1}$$

In this case, the voltage gain is as shown in (2)

$$\begin{aligned} A_v = \frac{V_o}{V_i} &= \left(1 - \frac{\omega^2 LC}{2} + j\omega\sqrt{LC}\sqrt{1 - \frac{\omega^2 LC}{4}}\right)^{-1} \\ &= \left(\frac{j\omega\sqrt{LC}}{2} + \sqrt{1 - \frac{\omega^2 LC}{4}}\right)^{-2} \\ &= \left(\sqrt{1 - \frac{\omega^2 LC}{4}} - \frac{j\omega\sqrt{LC}}{2}\right)^{2}. \end{aligned} \tag{2}$$

The cutoff frequency for this system is ω_c such that the discriminant ($1 - \omega^2 LC/4$) equals zero, and is as shown in (3)

$$\omega_c = \frac{2}{\sqrt{LC}}. \tag{3}$$

If there are n cascaded π-sections, as shown in Fig. 2(b), the overall voltage gain would be as shown in (4), where L is a function of n as shown in (5)

$$A_v = \frac{V_o}{V_i} = \left(\sqrt{1 - \frac{\omega^2 L(n) C}{4n}} - \frac{j\omega\sqrt{L(n)\frac{C}{n}}}{2}\right)^{2n} \tag{4}$$

$$L(n) = \frac{4nCZ_o^2}{4n^2 + (\omega_o C Z_o)^2} \tag{5}$$

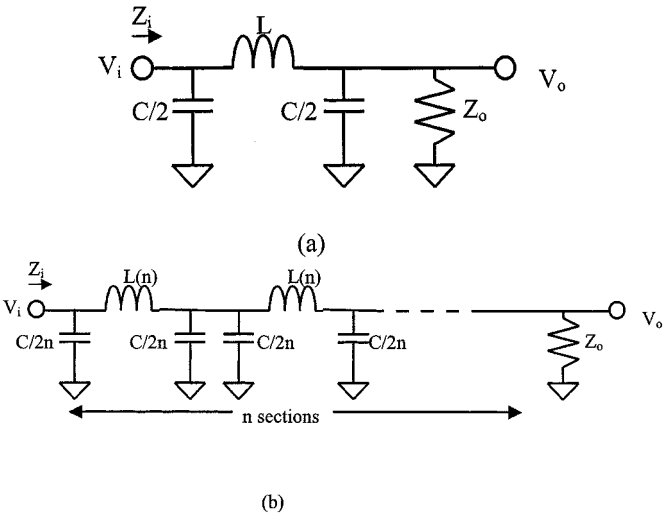

Fig. 2. (a) LC single π-section forming an artificial transmission line. L is chosen such that Z_i equals Z_o at the frequency of interest. (b) n-section transmission line, with the same total capacitance as (a). L is a nonlinear function of n in this case.

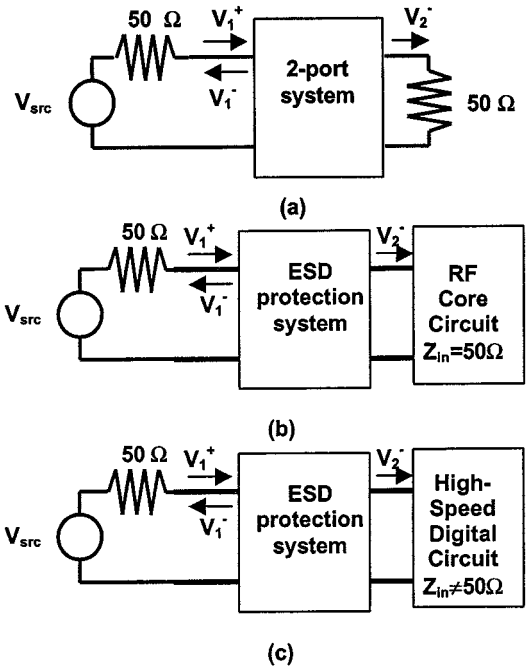

Fig. 3. (a) General 50 Ω two-port system showing the incident, reflected and transmitted voltages. The 50 Ω voltage source (V_{src}) drives the system, and after passing through the two-port system, power is transferred to the 50 Ω load at the right. (b) Two-port model of an RF system with an ESD protection system. Note the analogy between (a) and (b). (c) With a high-speed digital circuit as the load, the impedance of the load is no longer at 50 Ω, and the situation differs from that of (a) and (b).

Substituting (5) into the discriminant from (4) and equating that to zero yields the cutoff frequency shown in (6)

$$\omega_c = \sqrt{\frac{4n^2 + \omega_o^2 Z_o^2 C^2}{Z_o^2 C^2}}. \tag{6}$$

As can be seen, with increasing n, the cutoff frequency of the transmission line increases. Thus for a known capacitance, as determined from the ESD requirement, dividing the capacitive

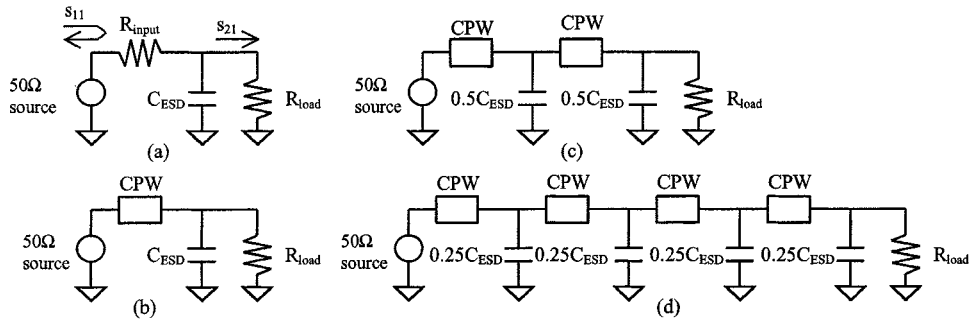

Fig. 4. (a) Equivalent circuit with a general ESD protection device between the source and the load. (b) A length of CPW is added to the previous circuit, to improve impedance matching. (c) Two-section transmission line structure formed by CPW and the protection devices. (d) Four-section transmission line structure.

loading into sections allows operation at a higher frequency under normal conditions.

It is instructive to note that with increasing number of sections, the capacitance associated with each section, $(C/2n)$, decreases, which will require smaller ESD protection devices between the transmission line sections. As the size of these devices decreases, there is some concern regarding their effectiveness. However, in [15], it was shown that smaller NMOS ESD protection devices are more robust since they conduct current more uniformly, while as the protection devices become large, current flows through only a small section of the device, giving rise to smaller failure currents per unit transistor width. Additionally, in [8], ESD measurements of a distributed protection system was performed, whereby it was shown that each smaller element of the distributed protection scheme does indeed turn on under human body model (HBM) and charged device model (CDM) stress. Although the above mentioned results lend strong support to the distributed ESD protection scheme, the impact of this protection scheme on the RF signal under normal operation has not been quantified. The following sections show the effect of such ESD protection on high-speed signals and propose a methodology for designing optimal distributed ESD protection systems to minimize their effects on the integrity of high-speed signals.

III. S-Parameter Performance Analysis

In RF systems, the s-parameter matrix is often used to represent the characteristics of the network. As the system operating frequency increases such that the wavelength becomes comparable to the device dimensions, the wave-nature of signal propagation cannot be ignored. Also, generating pure open and short loads to calibrate the network measurement equipment becomes increasingly difficult at higher frequencies, as small parasitics greatly affect the impedances. The s-parameter matrix, which consists of ratios of outgoing to incoming signals measured with resistive terminations at each network port, satisfies the requirements for accurate high-frequency characterization [16]. Most often, RF networks are standardized to 50 Ω input and output impedances for maximum power transfer. S-parameter measurements are then taken as the reflection at, and transmission between ports with 50 Ω termination at each port.

Fig. 3(a) shows the measurements required for a general two-port system. When a voltage is applied from a 50 Ω source (V_{src}), the ratio of the reflected signal to the incident signal is the input reflection s-parameter, s_{11}, which is also equal to the reflection coefficient Γ as shown in (7)

$$s_{11} = \frac{V_1^-}{V_1^+} = \Gamma \tag{7}$$

$$s_{21} = \frac{V_2^-}{V_1^+}. \tag{8}$$

The forward transmission s-parameter, s_{21}, is the ratio of the outgoing signal at port 2 to the incident signal at port 1 as shown in (8). These two parameters characterize how much signal is reflected by the system, and how much signal is transmitted to the 50 Ω load. Often, s_{11} is plotted on a Smith Chart, which is a diagram that allows representation of reflections and impedances [17]. Looking at the Smith Chart as a polar plot corresponds to looking at reflections, while the various arcs of the Smith Chart represent lines of constant resistance and reactance. Thus the magnitude of impedance mismatch and signal reflection may both be gleaned from Smith Chart plots.

A generalized RF system with an ESD protection network is shown in Fig. 3(b). S-parameters may be used to quantify the impact of the ESD protection system on the signal transmission between the input and the core circuit. The s_{11} of the ESD protection system shows how much signal is reflected back to the input, and s_{21} shows how much of the signal applied at the input reaches the core circuit. Thus the goal of the ESD protection circuit is to protect the core circuit while minimizing s_{11} and maximizing s_{21} of the system.

Since both the input and output impedances are standardized to 50 Ω in RF circuits, an analogous situation exists for ESD protection at the RF outputs. However, digital systems do not have standardized input and output impedances as shown in Fig. 3(c), therefore modifications are necessary in analyzing high-speed digital circuits, and this will be discussed in Section V.

Starting with a standard 50 Ω system as is commonly found in RF systems, four different implementations of ESD protection are investigated, as shown in Fig. 4. A 50 Ω signal source drives the input to the protection circuit, and the output of the protection circuit is connected to the system to be protected, as modeled by a 50 Ω load (R_{load}). In each circuit, the protection device is modeled as a capacitance and input resistance, and interconnects between the pin and ESD circuit or between distributed ESD elements are modeled by a resistance or a CPW. Initially, the capacitance is assumed to be 200 fF, a value sufficient to provide a 2 kV ESD protection level [2]. Fig. 4(a),

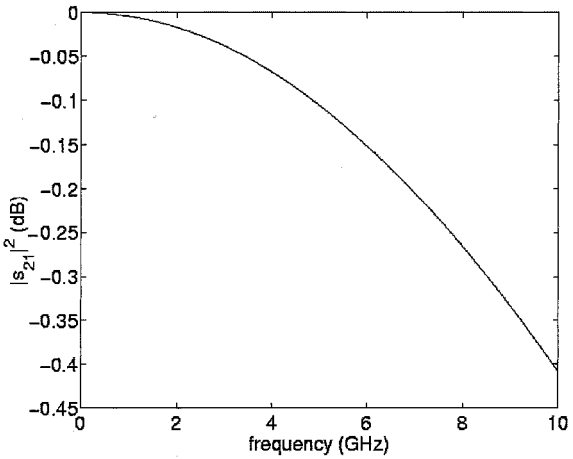

Fig. 5. Plot of signal power loss versus frequency for the circuit in Fig. 4(a), with an ESD device capacitance of 200 fF and R_{input} of zero.

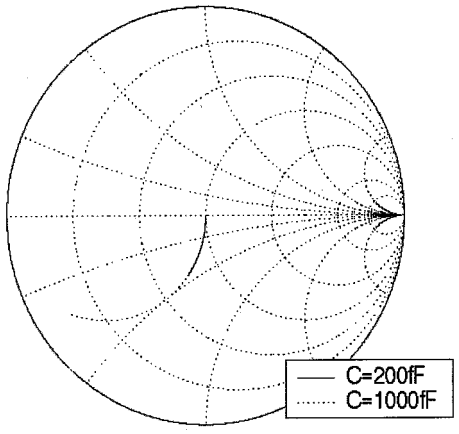

Fig. 6. Smith Chart representation of the effect of C_{ESD} on s_{11} for Fig. 4(a), with zero series resistance ($R_{input} = 0$) at $f = 10$ GHz.

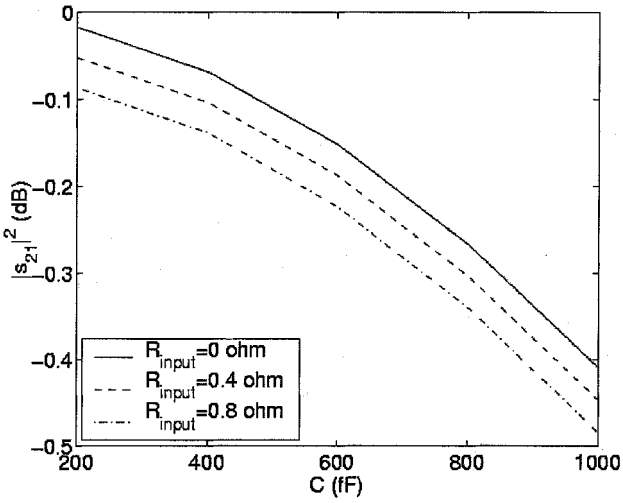

Fig. 7. Performance versus capacitance with varying R_{input} for Fig. 4(a) at $f = 2$ GHz. Note the increase in loss with increased resistance.

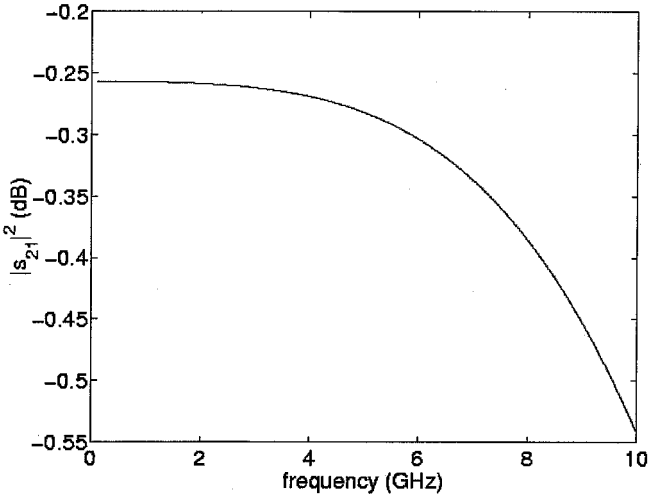

Fig. 8. Plot of signal power loss versus frequency for Fig. 4(b), with $C_{ESD} = 200$ fF.

which represents the most general ESD protection, consists of the source, load, a resistor representing interconnect and device loss (R_{input}), and the protection device and pad parasitic capacitance (C_{ESD}). Fig. 4(b) introduces a CPW between the source and the protection device to provide a better impedance match. The required CPW length was calculated using Smith Charts and impedance transformations to minimize reflections. This methodology is discussed in detail in Section VI. Fig. 4(c) and 4(d) show series circuits with smaller sections for better broadband match as the circuit approaches an ideal transmission line made of infinitesimal sections. For the purpose of this study, transmission lines with a maximum of four sections were examined. Although more sections may yield better performance, any further gain would be marginal. Also, the added complexity of having more sections may be undesirable, and depending on the layout topology, it may be unreasonable to further divide the ESD device and pad capacitances into smaller elements. S-parameter simulations over the frequency range 0–10 GHz were performed on these circuits using the microwave circuit simulator ADS [18], to generate the reflection parameter s_{11}, and the transmission parameter s_{21}. As shown in Fig. 4(a), s_{11} corresponds to the amount of signal that is reflected at the input, and s_{21} corresponds to the amount of input signal that reaches the load. The objective of the system designer is to minimize s_{11} and maximize s_{21}. This study uses $|s_{11}|^2$ and $|s_{21}|^2$ as performance metrics since these coefficients are then directly proportional to power.

Next, the simulations are repeated for a set of capacitances, thus modeling different protection devices with different protection levels. The data from these simulations can be used to provide designers with insight into how much complexity is required in the protection system to obtain the desired ESD protection along with sufficient high-speed performance at the operating frequency of interest.

IV. Results and Discussion

Fig. 5 shows the results from the simulation of the simplest case from Fig. 4(a), with the input resistance set to zero and $C_{ESD} = 200$ fF. Since the whole system is lossless, all the power loss is due to signal reflection caused by impedance mismatch. While most of the power reaches the load at low frequencies, the capacitance loads the circuit at higher frequencies.

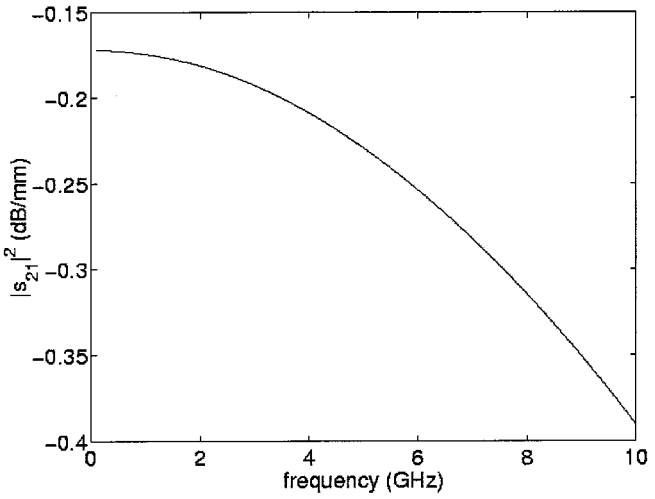

Fig. 9. CPW loss per mm versus frequency, showing the inherent loss found in the CPW due to resistive and dielectric loss.

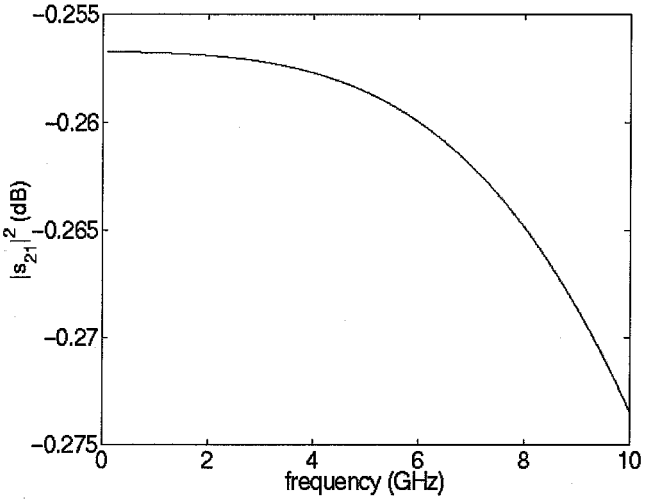

Fig. 11. Plot of signal power loss versus frequency for Fig. 4(d), with $C_{ESD} = 200$ fF. The loss is now less than 0.275 dB at 10 GHz.

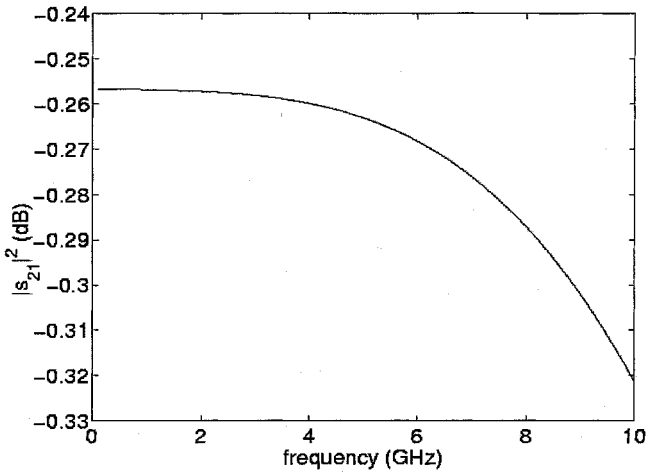

Fig. 10. Plot of signal power loss versus frequency for Fig. 4(c), with $C_{ESD} = 200$ fF. Note the better loss characteristics compared to Fig. 8.

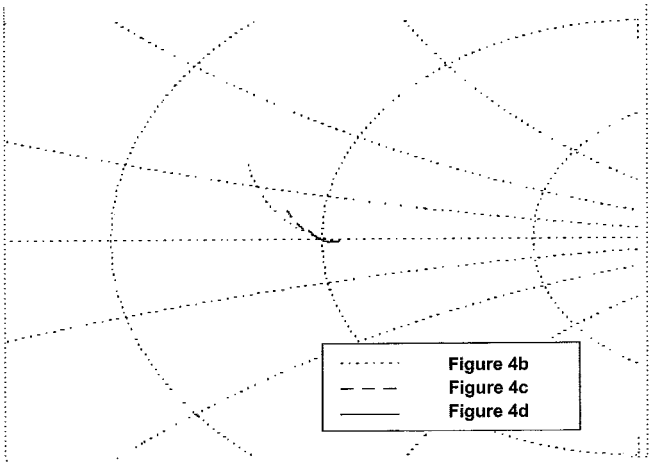

Fig. 12. Smith chart representation of s_{11} for Fig. 4(b) to 4(d), over the frequency range 0–10 GHz, with $C_{ESD} = 200$ fF. The reflection decreases with increasing number of sections.

Using a larger protection device in the same circuit gives s_{11} like that in Fig. 6. On this Smith Chart, it can be observed that the magnitude of the reflection increases with increased capacitance, thus less power is delivered to the load. Also, with increasing input resistance, the loss increases, as shown in Fig. 7.

The effect of employing CPWs in the ESD protection is also examined. Fig. 8 corresponds to the circuit in Fig. 4(b), where a CPW with a characteristic impedance of 100 Ω as determined by appropriate physical parameters of the transmission line such as width, thickness, spacing, dielectric constant, and loss tangent, is added to provide some impedance match. In the case of Fig. 8, the loss is due to the CPW loss and the mismatch loss. With a CPW length of 1.3 mm, there is a 0.25 dB loss even at low frequencies. As shown in Fig. 9, this CPW has a loss of 0.18 dB/mm at low frequencies, with the loss becoming worse with increased frequency, to 0.39 dB/mm at 10 GHz. At higher frequencies, this CPW loss worsens, while the mismatch loss also becomes larger. Comparatively, this result is worse than that of Fig. 5, but since Fig. 5 shows an ideal case where there is no resistive loss at all, this is to be expected. Note that if the CPW were lossless, the results with the CPW would be better than that of Fig. 5.

Figs. 10 and 11 show the results from simulating the circuit in Fig. 4(c) and 4(d), respectively. The losses observed are less than those seen in both Figs. 5 and 8 at higher frequencies. At low frequencies, the CPW losses are again observed. Fig. 11 shows loss characteristics that decrease by less than 0.02 dB between 0 and 10 GHz, with the maximum loss of 0.273 dB at 10 GHz, thus demonstrating good broadband characteristics.

Fig. 12 shows the reflection parameter s_{11} corresponding to Fig. 4(b) to 4(d). Note that the reflection observed becomes smaller with increased number of CPW sections.

The impact of the protection level is analyzed next by varying the size of the protection device (C_{ESD}). Figs. 13–16 plot the power loss as represented by $|s_{21}|^2$ in the protection systems in Fig. 4 against the parasitic capacitance posed by the protection devices. It is clear that higher frequencies and larger capacitances generate larger losses. The ideal case ($R_{input} = 0$) in Fig. 13 shows that at low frequencies, the loss is minimal irrespective of the device capacitance. The single CPW case

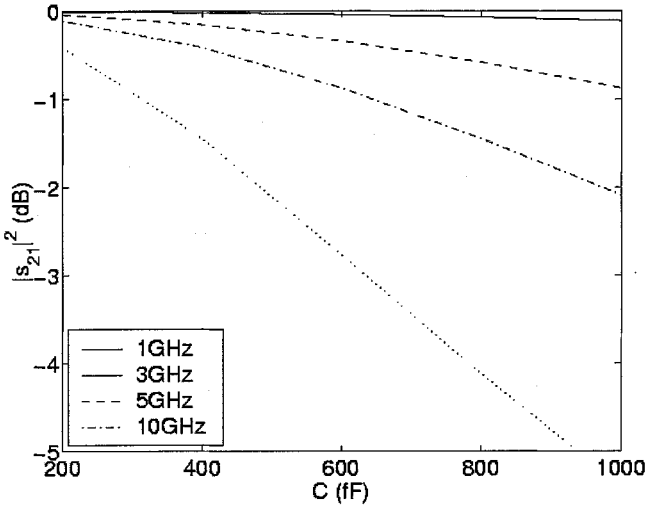

Fig. 13. Signal power loss versus parasitic capacitance for a set of frequencies for the circuit in Fig. 4(a).

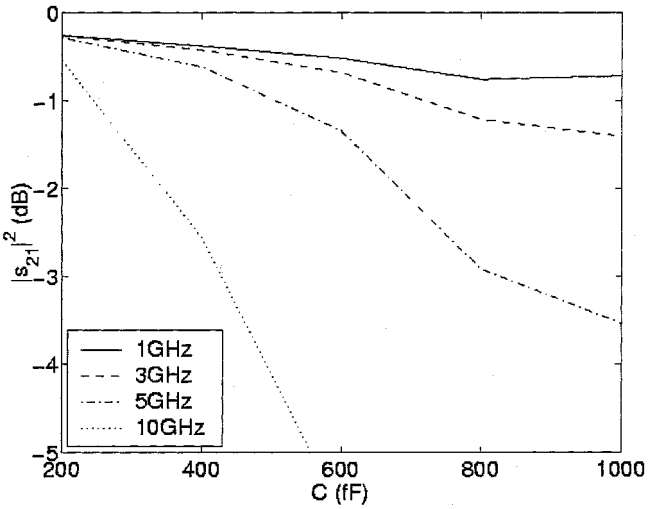

Fig. 14. Performance versus capacitance plot for the circuit in Fig. 4(b).

of Fig. 14 shows resistive loss in the CPW, resulting in poor performance at all frequencies. However, a more distributed protection system can minimize the loss for a wider frequency range, as shown in Figs. 15 and 16. Also, Fig. 16, which represents the four-segment distributed protection, shows that the loss will only vary by 0.85 dB for all capacitances, thus showing immunity to variations in ESD device depletion capacitance due to changes in dc bias levels.

The above results indeed show that dividing the ESD protection device into a few smaller sections provides better broadband RF performance. But for high-speed digital systems, there are differences in the circuit characteristics that prevent the use of s-parameter analysis. These differences are addressed, and a solution toward designing effective distributed ESD systems, even in a high-speed digital environment, is proposed in the next section.

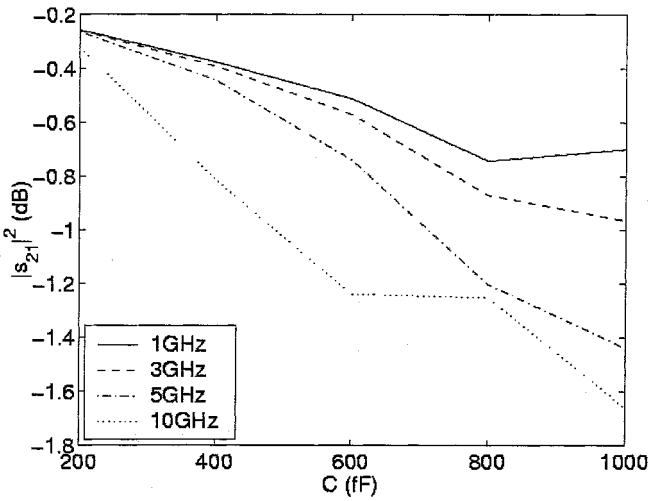

Fig. 15. Performance versus capacitance plot for the circuit in Fig. 4(c). Note that the curves start to converge for all frequencies.

V. Modifications for Applications to High-Speed Digital Circuits

In the case of high-speed digital circuits, the impedance termination conditions are not as well defined as in the RF case. Input buffers present a capacitive load due to the gate capacitance of the devices, and output buffers present a capacitance due to the drain junction capacitance in parallel with the on-resistance (R_{on}) of the conducting device. These terminal impedances vary depending on the buffer sizes and voltage levels, and therefore transmission and reflection from a transmission line would also vary.

In order to facilitate the design of the distributed ESD protection system, we propose terminating these digital terminals resistively, as suggested in [19]. By applying a 50 Ω termination resistor for the input buffer as shown in Fig. 17(a), and for the output buffer as shown in Fig. 17(b), s-parameter analysis may then be performed on these digital circuits as well. The capacitances presented by the buffer transistors themselves may be absorbed into the ESD protection system capacitance for design purposes.

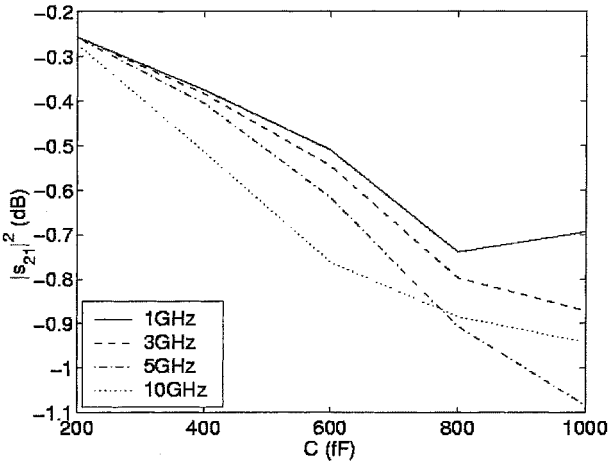

Fig. 16. Performance versus capacitance plot for the circuit in Fig. 4(d). Note that the variation of the loss over all measured frequencies and capacitances is only 0.85 dB.

In addition to allowing s-parameter analysis, application of termination resistances prevents intersymbol interference

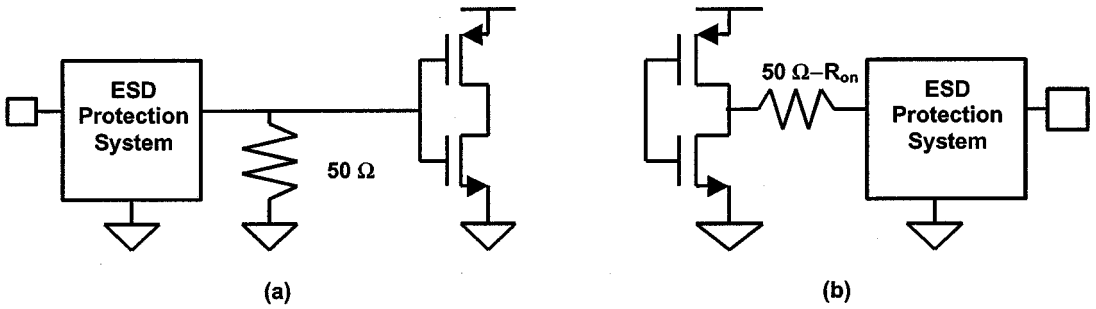

Fig. 17. (a) Modified high-speed digital input buffer with a 50 Ω parallel resistive termination to prevent reflections. (b) Output buffer with a series resistive termination. Note that the series termination resistor would be less than 50 Ω depending on R_{on}, but since R_{on} should be small for a well-designed device, 50 Ω is a good approximation for the termination resistance.

(ISI) by not generating any reflections at the terminals. Also, crosstalk that generates reverse-traveling noise will no longer affect the forward-traveling signal because of proper termination at the terminals. The price that is paid for these benefits is additional die area, and perhaps an increase in power consumption.

With 50 Ω terminations both in RF and high-speed digital systems, effective signal transmission may be achieved by applying a distributed ESD protection system. Thus the next section will demonstrate methodologies for designing distributed ESD protection systems.

VI. Design Methodologies for Optimized Distributed ESD Protection

Prior to determining the proper CPW characteristics, three parameters must be fixed. They are the maximum operating frequency $f_{\max}$, the equivalent ESD capacitance C_{ESD}, and the CPW characteristic impedance Z_{CPW}. Selecting $f_{\max}$ should consist only of determining the maximum frequency specification for the core circuit. C_{ESD} should be calculated after determining the proper ESD device size required for a particular protection level in a given technology. The equivalent capacitance may then be calculated from the device junction areas, or obtained through simulations.

The appropriate dimensions for the CPW as shown in Fig. 18 must then be determined. The minimum width (W) must be such that given a line thickness (t), which is technology dependent, the maximum possible ESD current can flow without causing open circuit failure of the line. An analytical model for the calculation of this width is provided in [20]. The distance between the substrate and the metal lines (d) is also technology dependent, but in general, the CPW should be placed as far away from the substrate as possible to reduce loss. The substrate resistivity also affects loss as shown in [21], where it is shown that CPW on low-resistivity substrates suffers greater loss than CPW on high-resistivity substrates.

Once the minimum CPW signal line width is defined, the signal-to-ground spacings (s) of the CPW need to be determined from the desired characteristic impedance. In general, high characteristic impedance is desirable to minimize the required CPW length, but losses, which tend to be higher for higher impedance lines, need to be minimized. The exact relationship between W, s, d, t, Z_{CPW}, substrate characteristics, and loss is a complex one that is beyond the scope of this study.

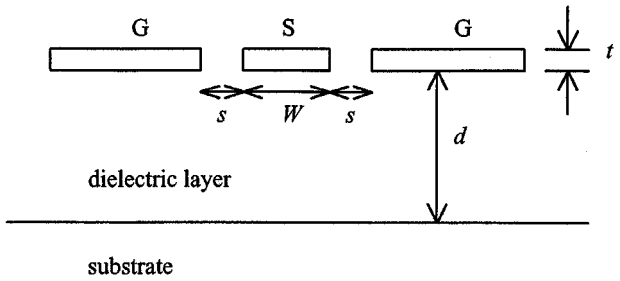

Fig. 18. Cross section of a coplanar waveguide (CPW). The lines are configured ground-signal-ground (G-S-G), with the key dimensions being the line width W, the spacing s, the CPW thickness t, and the distance of CPW from substrate d.

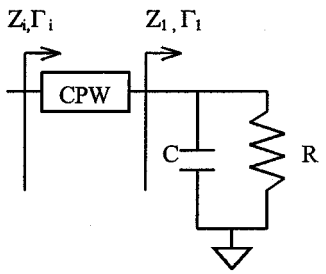

Fig. 19. Circuit diagram for the example calculation in Section VI. $R = 50\ \Omega$ and $f = 10$ GHz. The values of C and lengths of CPW vary. The impedances (Z) and reflection coefficients (Γ) are used to calculate the optimal C, CPW length, and number of distributed sections.

In this work, a high characteristic impedance CPW line described in [22] is used. This CPW was fabricated on a low-resistivity (0.5 Ω-cm) substrate, with an aluminum (Al) metal layer 8 μm above the substrate: a distance typical for global interconnects. At present, VLSI metallization is realized with copper (Cu) which has higher electrical conductivity than Al [23], resulting in lower conductor loss. The CPW loss characteristics were measured in [22], and for this work, the ADS CPW model parameters were adjusted so that the loss characteristic of the model is similar to the experimentally measured loss. This loss characteristic is shown in Fig. 9.

For the following example, $f_{\max}$ was set at 10 GHz, C_{ESD} was chosen to be 200 fF for a 2 kV protection level [2], and Z_{CPW} was chosen to be 100 Ω, a high-impedance, low-loss line according to [22]. For simulation in ADS, the transmission line has a thickness of 2 μm, $W = 5\ \mu$m, and $s = 10\ \mu$m. Along with calculating the CPW length, the number of distributed sections to be created is also determined. The equivalent circuit used

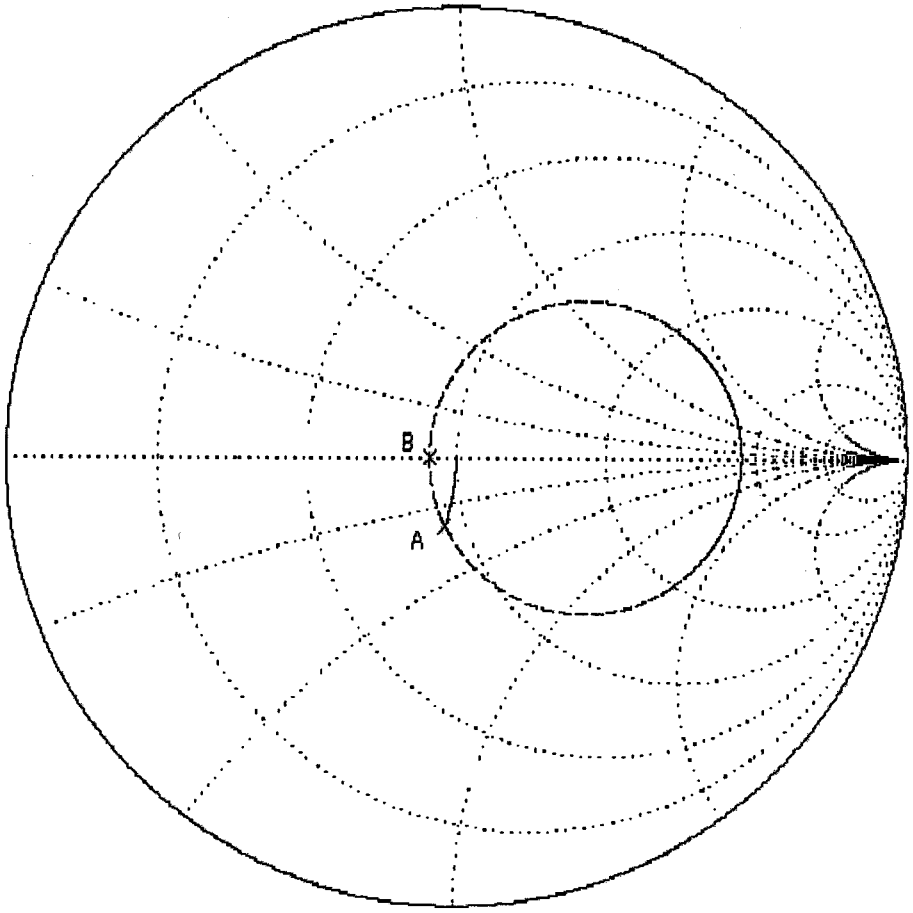

Fig. 20. The 50 Ω-normalized Smith chart. Point A shows Γ_1 for 200 fF at 10 GHz. Point B shows Γ_i. The dotted circle shows the locus for different lengths of CPW.

to achieve this is shown in Fig. 19. First, factors of the ESD capacitance are determined (in this case, 200 fF, 100 fF, 67 fF, 50 fF, 40 fF…) and are represented in the circuit as C. Then Z_1 is determined for each capacitance at $f_{\max}$, and R is the 50 Ω load resistance. These impedances correspond to points on arc A on the Smith Charts (Figs. 20 and 21). From the impedance Z_1, the reflection coefficient Γ_1 is calculated using the formula given by (9)

$$\Gamma_1 = \frac{Z_1 - Z_{CPW}}{Z_1 + Z_{CPW}}. \tag{9}$$

Gamma, like s_{11}, represents the coordinate on the Smith Chart planes in Figs. 20 and 21, with the center as the origin and the outside circle being unity. Converting Γ_1 into polar coordinates gives the magnitude ρ and phase ϕ. By adding some length of CPW, we attempt to bring the phase to 180° (point B). For a CPW with characteristic impedance of Z_{CPW}, the locus that results from adding CPW to Z_1 is a circle centered about the origin in Fig. 21 (the dotted circle). Note that when this is viewed on a Smith Chart normalized to 50 Ω, the circle is not centered at the origin (Fig. 20). Since a full circle around requires a CPW which is a half-wavelength ($\lambda/2$), the correct CPW length can be calculated from (10)

$$\text{CPW length} = \frac{|\phi - \pi|}{2\pi}\frac{\lambda}{2}. \tag{10}$$

Adding the correct CPW length should yield Γ_i with magnitude $\rho_i = \rho$ and $\phi_i = 180°$. This can then be transformed into impedance with (11).

$$Z_i = \frac{(1+\Gamma_i)}{(1-\Gamma_i)} Z_{CPW}. \tag{11}$$

As a measure of how close Z_i comes to the system impedance (Z_o) of 50 Ω, the standing wave ratio (SWR) can be calculated, as shown in (12)

$$SWR = \frac{1 + \left|\frac{Z_i - Z_o}{Z_i + Z_o}\right|}{1 - \left|\frac{Z_i - Z_o}{Z_i + Z_o}\right|}. \tag{12}$$

A Z_i of 50 Ω results in an SWR of unity, and the closer the SWR is to unity, the better the match that is obtained. All the values calculated for this example are summarized in Table I.

Now given the ESD capacitance and the maximum allowable SWR, the number of sections required to achieve those specifications can be readily calculated using the methodology mentioned previously. Note that this is valid because $R = 50\,\Omega$, and we try to bring Z_i to 50 Ω for each section. Thus the next section to be added can regard Z_i of the present section as just a 50 Ω load. However, if the capacitance of the section is large, the resulting SWR of the section will also be large, meaning that the Z_i of each section will not be equal to 50 Ω. In this

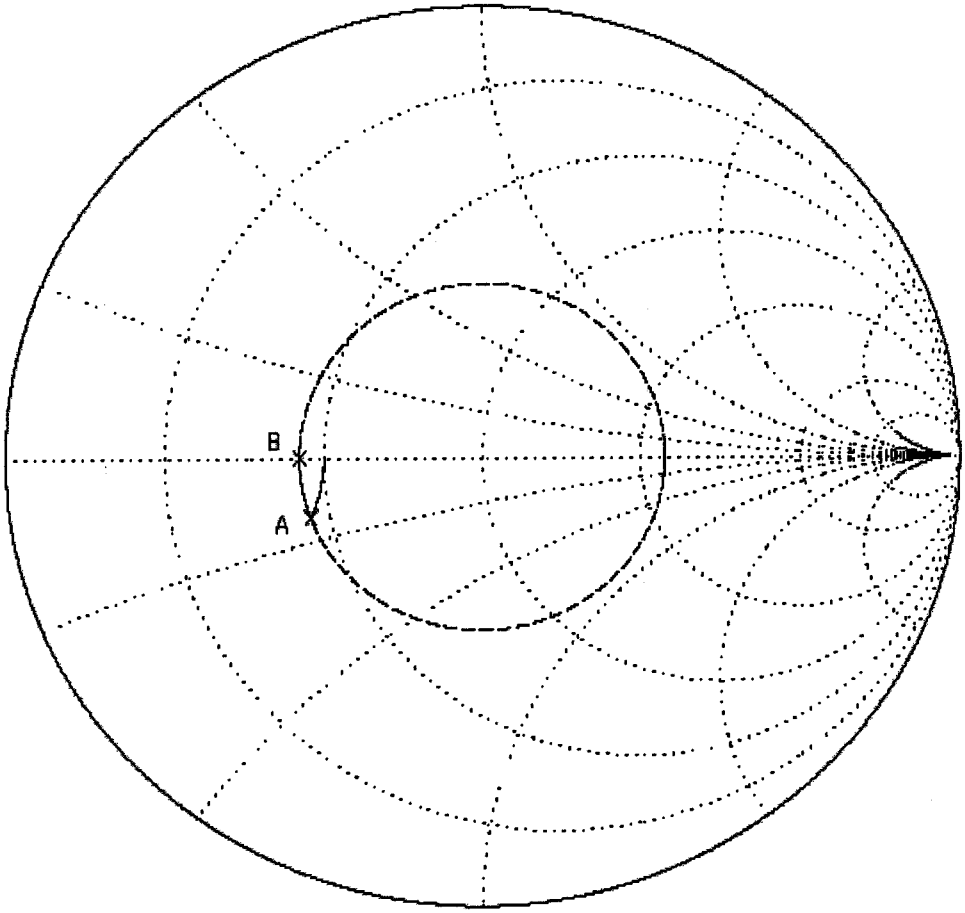

Fig. 21. The 100 Ω-normalized Smith chart. Point A shows Γ_1 for 200 fF at 10 GHz. Point B shows Γ_i. The dotted circle shows the locus for different lengths of CPW.

TABLE I
SUMMARY OF RESULTS FROM THE EXAMPLE CASE. NOTE THAT WITH INCREASED SECTIONS, Z_i AND SWR APPROACH 50 Ω, AND 1.00, RESPECTIVELY

C (fF)	# sections	Z_1 (Ω)	Γ_1	ρ	ϕ (rad)	Arc length $\lvert\phi-\pi\rvert$ (rad)	Z_i (Ω)	SWR
200	1	35.85-22.52j	-0.43-0.24j	0.494	-2.64	0.502	33.9	1.48
100	2	45.51-14.30j	-0.36-0.13j	0.385	-2.79	0.355	44.4	1.13
67	3	47.88-10.08j	-0.35-0.092j	0.358	-2.88	0.259	47.3	1.06
50	4	48.80-7.66j	-0.34-0.069j	0.348	-2.94	0.200	48.4	1.03
40	5	49.22-6.19j	-0.338-0.056j	0.343	-2.98	0.163	49.0	1.02

case, error is introduced in the calculations, and this error is compounded when multiple sections, each with large SWR, are cascaded. While this error may be somewhat mitigated by the series resistance found in the transmission line, if the SWR of a single section is large, then the system SWR may be larger than suggested by the simple calculations. But since this methodology has decreased accuracy only when the SWR is large, which is undesirable anyway, the calculation results should be acceptable as long as the SWR of each section is close to unity.

One last consideration is to determine whether this analysis, performed for a system operating at $f_{\max}$, is valid when the system operates at a frequency lower than $f_{\max}$. It can be shown that at a lower frequency, the capacitance has a larger impedance. Thus, the arc on the Smith Chart becomes shorter, and ρ decreases, resulting in a smaller SWR. Thus, the $f_{\max}$ case is the worst case, and if the performance there is satisfactory, then the performance at any lower frequency will be at least as good as that seen at $f_{\max}$.

While the previous methodology relies on some geometrical concepts regarding the Smith Chart, there is an alternate, more mathematical methodology by which the same results may be obtained. This methodology uses $ABCD$-matrices, which, like the s-parameter matrix, is a matrix set that describes the characteristics of a two-port network. The $ABCD$-matrix has the characteristics that when multiple two-port networks are cascaded, the system response is characterized by the product of the $ABCD$-matrices of the component two-port networks. This property of $ABCD$-matrices can also be used to calculate the correct CPW length. The general form of the $ABCD$-matrix

for a transmission line with characteristic impedance Z_{o1} and length l, and for a shunt impedance Z, are shown in (13) and (14), respectively

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos\frac{2\pi}{\lambda}l & j\frac{Z_{o1}}{Z_o}\sin\frac{2\pi}{\lambda}l \\ j\frac{Z_o}{Z_{o1}}\sin\frac{2\pi}{\lambda}l & \cos\frac{2\pi}{\lambda}l \end{bmatrix} \tag{13}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{Z_o}{Z} & 1 \end{bmatrix}. \tag{14}$$

In our example, the system impedance Z_o is 50 Ω, while Z_{o1} is 100 Ω. Looking again at Fig. 19, the cascading of the CPW with the shunt impedance Z_1 gives the $ABCD$-matrices for the system as shown in (15)

$$\begin{bmatrix} A_i & B_i \\ C_i & D_i \end{bmatrix} = \begin{bmatrix} \cos\frac{2\pi}{\lambda}l & j2sin\frac{2\pi}{\lambda}l \\ j0.5\sin\frac{2\pi}{\lambda}l & \cos\frac{2\pi}{\lambda}l \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ 50\left(\frac{1}{R}+j\omega C\right) & 1 \end{bmatrix}. \tag{15}$$

The product of the $ABCD$-matrix for the CPW and for the parallel RC combination gives the system response looking into the input terminal, as denoted by the subscript i. From the product, the input impedance Z_i may be calculated by taking A_i/C_i of the matrix. By setting the imaginary component of this impedance to zero, since we desire the impedance to be a resistance close to 50 Ω, the CPW length may be calculated to be as shown in (16).

$$\frac{l}{\lambda} = \frac{1}{4\pi}\tan^{-1}\frac{2Z_o\omega C}{\frac{Z_{o1}}{Z_o}\left(\left(\frac{Z_o}{R}\right)^2+\left(Z_o\omega C\right)^2\right)-\frac{Z_o}{Z_{o1}}}. \tag{16}$$

Using this length, the input resistance R_i may be calculated as shown in (17)

$$R_i = \frac{\frac{Z_o^2}{R}}{\left(\frac{Z_o}{R}\right)^2\cos^2\left(\frac{2\pi}{\lambda}l\right)+\left(\frac{Z_o}{Z_{o1}}\sin\left(\frac{2\pi}{\lambda}l\right)+\omega CZ_o\cos\left(\frac{2\pi}{\lambda}l\right)\right)^2}. \tag{17}$$

Repeating the calculations for the different capacitances using $ABCD$-matrices yields results identical to those obtained using the Smith Chart method.

VII. Conclusion

In conclusion, this paper has presented quantitative methodologies to analyze the performance degradation of RF and high-frequency mixed-signal circuits due to distributed ESD protection devices at I/O pads. Detailed s-parameter analysis of high-frequency systems has been carried out to illustrate the impact of the parasitics associated with distributed ESD protection schemes. Circuit simulations using coplanar waveguides to absorb a 200 fF parasitic capacitance of the ESD protection devices have shown that a four-stage distributed ESD protection system suffers only a 0.02 dB loss between 0–10 GHz, with a maximum loss of 0.273 dB at 10 GHz, showing excellent broadband characteristics. Two generalized design methodologies, using Smith Charts and ABCD-parameters, have been developed to optimize the number and length of coplanar waveguides separating the distributed ESD elements. For a parasitic capacitance of 200 fF, a four-stage distributed ESD protection can be designed with 0.4 rad of 100 Ω transmission line to give an SWR of 1.03 at 10 GHz. Furthermore, termination schemes have been proposed to allow this analysis to be applicable to high-speed digital and mixed-signal systems. This work illustrates the utility of the distributed ESD protection structure for high-frequency applications and provides design methods, which can be useful to ESD and I/O designers.

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